ECHO-BOARD 1.1

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CONTENT

Revision History

Document	Carrier	Description
1.0	1.0	New Product
1.0A	1.0	Remove Q13 - STBY_3V3 Power supply enable Remove R64 & R65 - External CODEC option Replace R133 to 100K - USB0 OTG ID pin CUT U10 power pin and connect it to 1.8V - Internal DMIC CUT U37 power pin and connect it to 1.8V - External DMIC Connect UART2 to Debug Port instead of UART1 Switch between LCD0 PWM and LCD1 PWM Disconnect CARRIER_PWR_ON_3V3 from U27 & U33 - VCC_5V & BASE_PER_3V3 EN pin Connect U33 enable pin to VCC_5V Remove R113, ? R112 change to 0R - External DMIC Add 220R PUs to ETH LEDs Replace U44 to VIC1241 - NCP715SQ18T2G Remove D33 Replace R136 to 10K - VRS0030
1.1		New Layout

For complete alternate function per pin
and specific SOM please refer to:
" " located at:
ftp://ftp.variscite.com/DART_Compatibility

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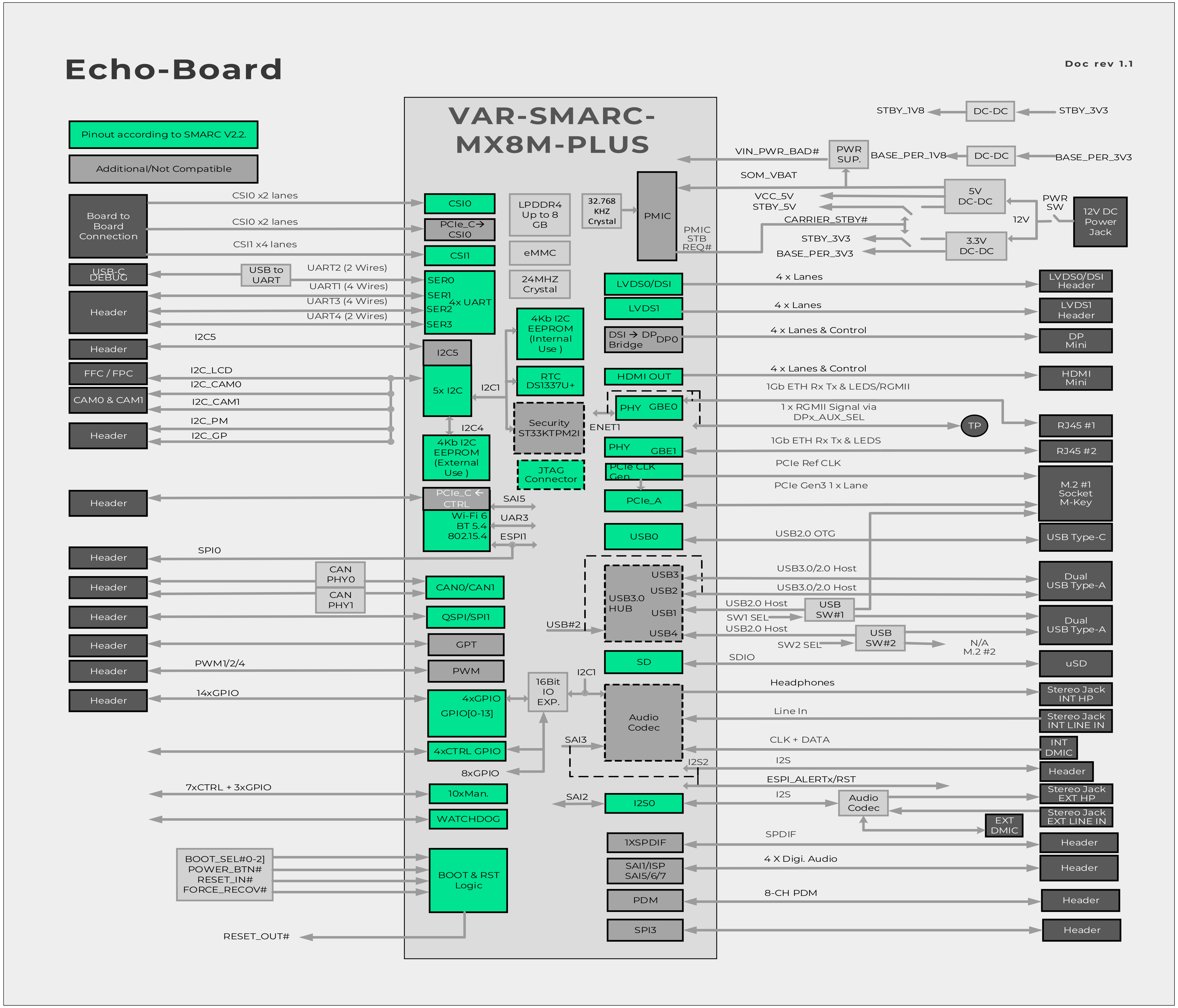
Title: 01. Cover			
Size: A3	Document Number: ECHO CUSTOMBOARD	Project: ECHO-BOARD	Rev: 1.1
Designer: Shay V.		Approved By:	
Date: Wednesday, January 21, 2026		Sheet 1 of 16	

02A. Block Diagram - VAR-SMARC-MX8M-PLUS



Echo-Board
Doc rev 1.1
Pinout according to SMARC V2.2.
Additional/Not Compatible
VAR-SMARC-MX8M-PLUS
Board to Board Connection
CSI0 x2 lanes
CSI0 x2 lanes
CSI1 x4 lanes
CSI0
PCIe_C → CSI0
CSI1
LPDDR4 Up to 8 GB
32.768 KHZ Crystal
PMIC
eMMC
24MHZ Crystal
USB-C DEBUG
USB to UART
UART2 (2 Wires)
UART1 (4 Wires)
UART3 (4 Wires)
UART4 (2 Wires)
SER0
SER1
SER2
SER3
4x UART
Header
I2C5
I2C5
FFC / FPC
I2C_LCD
I2C_CAM0
CAM0 & CAM1
I2C_CAM1
I2C_PM
I2C_GP
5x I2C
I2C1
I2C4
4Kb I2C EEPROM (Internal Use)
RTC DS1337U+
Security ST33KTPM2I
4Kb I2C EEPROM (External Use)
JTAG Connector
PCIe_C ← CTRL
Wi-Fi 6 BT 5.4 802.15.4
SAI5
UAR3
ESPI1
SPI0
CAN PHY0
CAN PHY1
CAN0/CAN1
QSPI/SPI1
GPT
PWM1/2/4
PWM
14xGPIO
4xGPIO
GPIO[0-13]
16Bit IO EXP.
4xCTRL GPIO
8xGPIO
7xCTRL + 3xGPIO
10xMan.
WATCHDOG
BOOT_SEL#0-2]
POWER_BTN#
RESET_IN#
FORCE_RECOV#
BOOT & RST Logic
RESET_OUT#
STBY_1V8
DC-DC
STBY_3V3
VIN_PWR_BAD#
PWR SUP.
BASE_PER_1V8
DC-DC
BASE_PER_3V3
SOM_VBAT
VCC_5V
STBY_5V
5V DC-DC
PWR SW
12V DC Power Jack
12V
CARRIER_STBY#
PMIC STB REQ#
STBY_3V3
BASE_PER_3V3
3.3V DC-DC
LVDS0/DSI
4 x Lanes
LVDS0/DSI Header
LVDS1
4 x Lanes
LVDS1 Header
DSI → DP Bridge
DP0
4 x Lanes & Control
DP Mini
HDMI OUT
4 x Lanes & Control
HDMI Mini
1Gb ETH Rx Tx & LEDS/RGMII
PHY GBE0
ENET1
1 x RGMII Signal via DPx_AUX_SEL
TP
RJ45 #1
PHY GBE1
1Gb ETH Rx Tx & LEDS
RJ45 #2
PCIe CLK Gen
PCIe Ref CLK
PCIe Gen3 1 x Lane
PCIe_A
M.2 #1 Socket M-Key
USB0
USB2.0 OTG
USB Type-C
USB3.0 HUB
USB3
USB2
USB1
USB4
USB#2
USB3.0/2.0 Host
USB3.0/2.0 Host
Dual USB Type-A
USB2.0 Host
SW1 SEL
USB SW#1
USB2.0 Host
USB SW#2
SW2 SEL
Dual USB Type-A
N/A M.2 #2
SD
SDIO
uSD
I2C1
Audio Codec
Headphones
Stereo Jack INT HP
Line In
Stereo Jack INT LINE IN
SAI3
CLK + DATA
INT DMIC
I2S2
I2S
Header
ESPI_ALERTx/RST
SAI2
I2S0
I2S
Audio Codec
Stereo Jack EXT HP
Stereo Jack EXT LINE IN
EXT DMIC
1XSPDIF
SPDIF
Header
SAI1/ISP SAI5/6/7
4 X Digi. Audio
Header
PDM
8-CH PDM
Header
SPI3
Header

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Title 02A. BD - VAR-SMR-MX8MP			
Size C	Document Number ECHO CUSTOMBOARD	Project ECHO-BOARD	Rev 1.1
Designer: Shay V.		Approved By:	
Date: Sunday, January 25, 2026		Sheet 2 of 16	

02B. Block Diagram - VAR-SMR-MX95 TBD

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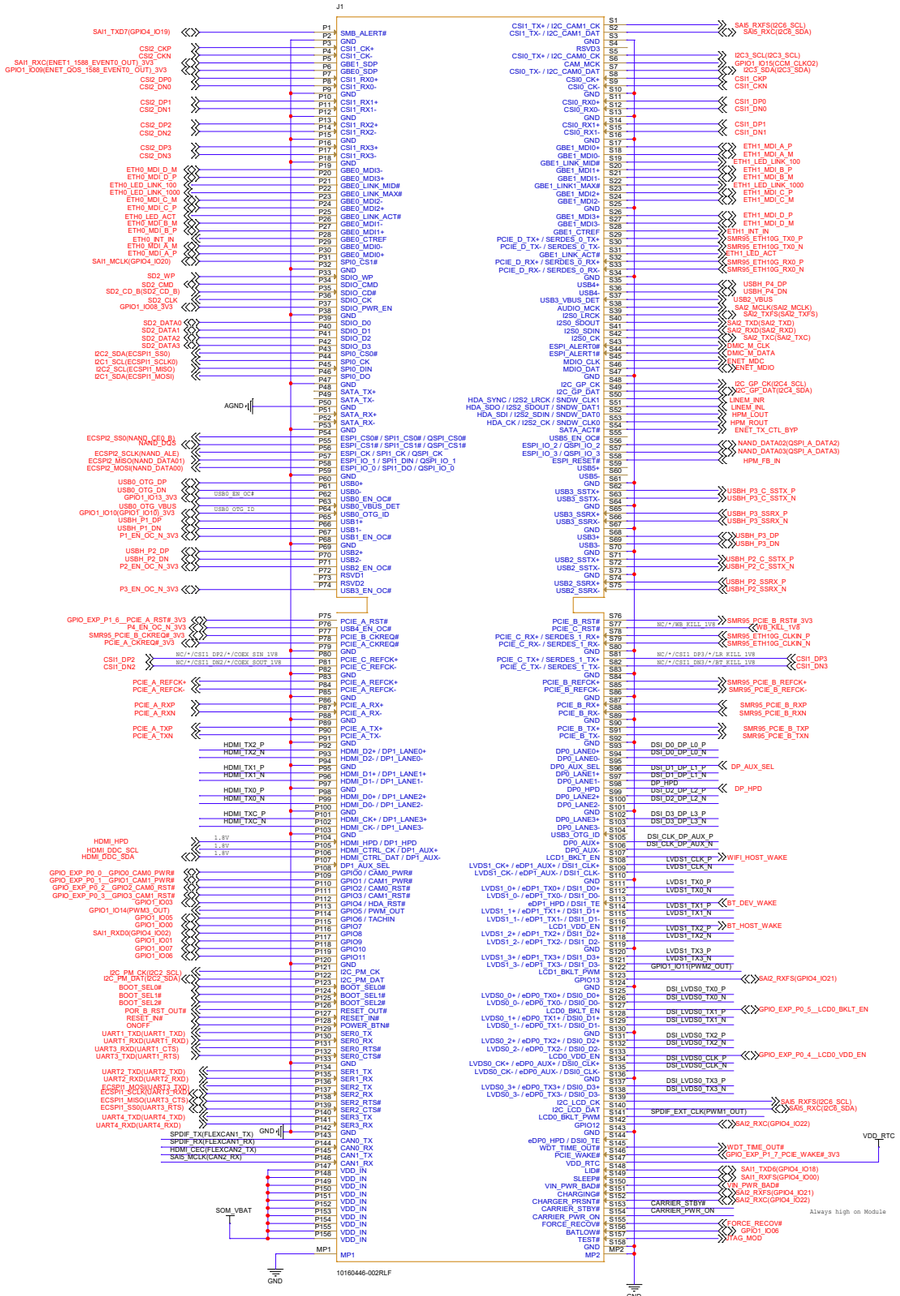
Title: 02B. BD - VAR-SMR-MX95			
Size: A3	Document Number: ECHO CUSTOMBOARD	Project: ECHO-BOARD	Rev: 1.1
Designer: Shay V.		Approved By:	
Date: Wednesday, January 21, 2026		Sheet 3 of 16	

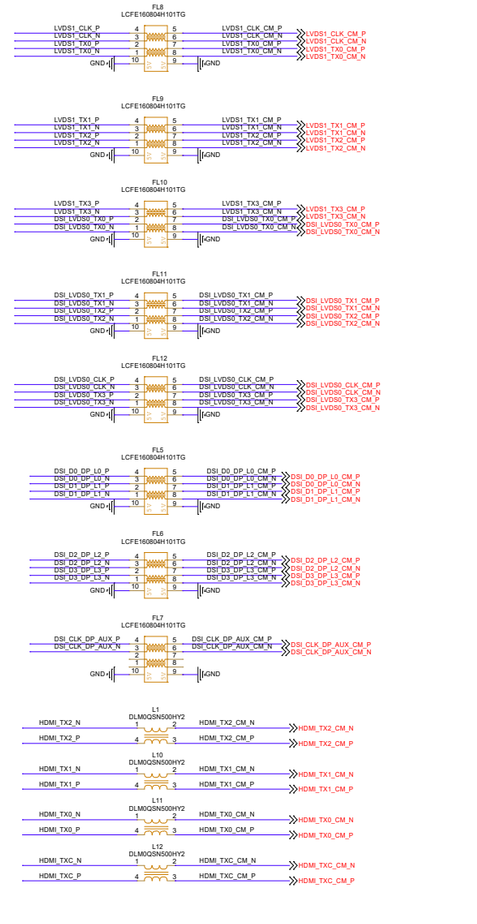
03A - VAR-SMR-MX8MP CONNECTOR



Level Shifters

EMI Filters & ESD Protection

Put close to SMARC connector



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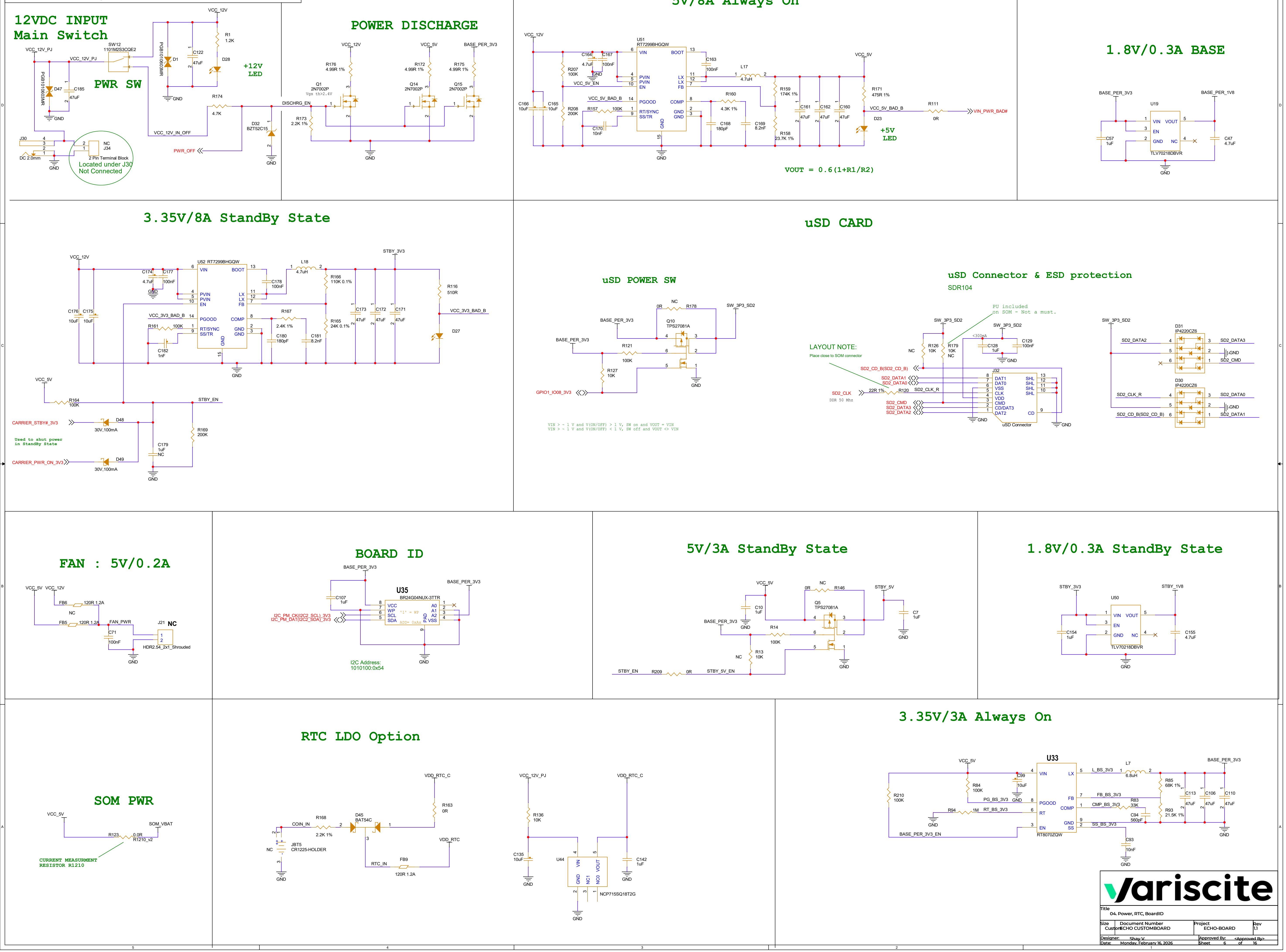
Title	03A. VAR-SMR-MX8MP		
Size A1	Document Number ECHO CUSTOMBOARD	Project ECHO-BOARD	Rev 1.3
Designer:	Shay V.	Approved By:	<Approved By>
Date:	Monday, February 16, 2026	Sheet 4 of 16	

03B - VAR-SMR-MX95 CONNECTOR TBD

Title: 03B. VAR-SMR-MX95			
Size: A2	Document Number: ECHO CUSTOMBOARD	Project: ECHO-BOARD	Rev: 1.1
Designer: Shay V.		Approved By:	
Date: Wednesday, January 21, 2026		Sheet 5 of 16	

04. Power, RTC & Board ID



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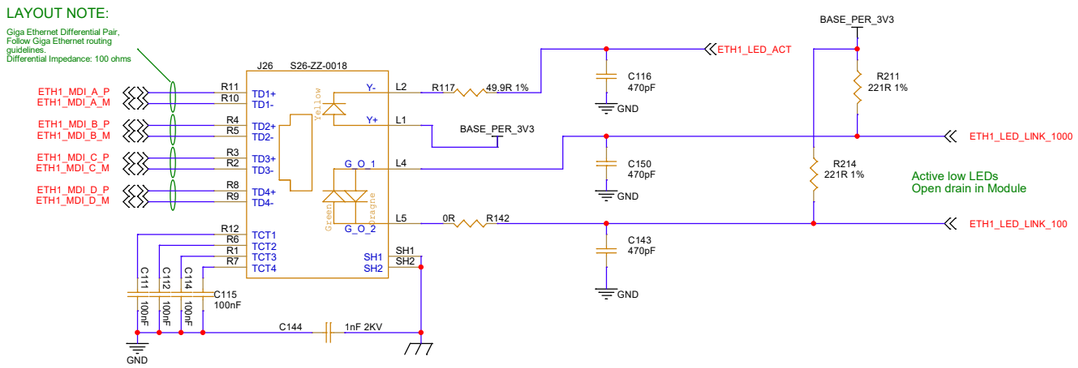
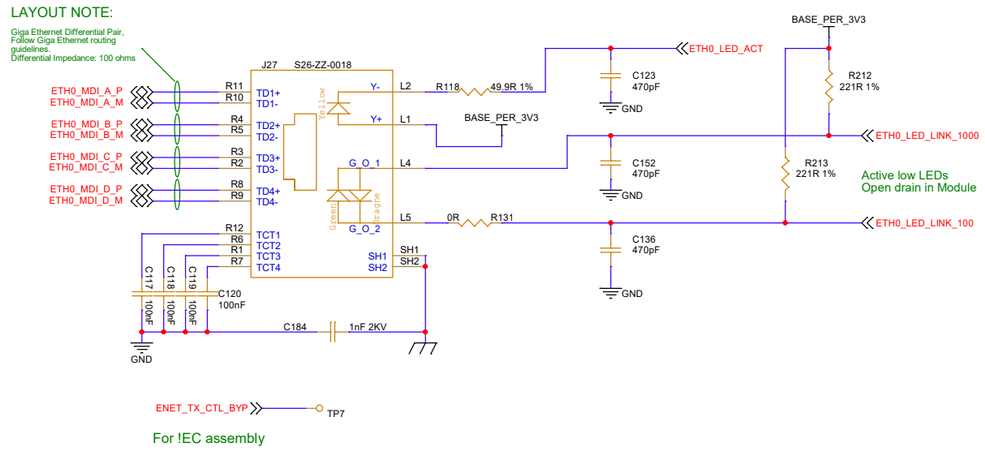
Title	04. Power, RTC, BoardID		
Size Custom	Document Number ECHO CUSTOMBOARD	Project ECHO-BOARD	Rev 1.1
Designer: Shay V.		Approved By: <Approved By>	
Date: Monday, February 16, 2026		Sheet 6 of 16	

05. ETHERNET

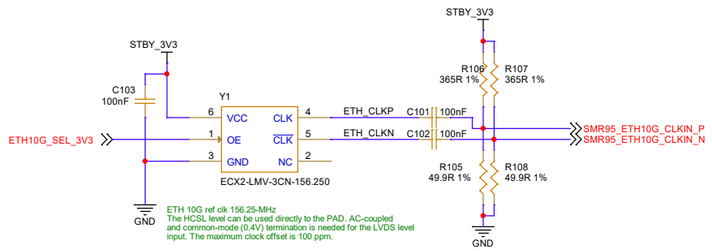
Gigabit Ethernet - ETH1

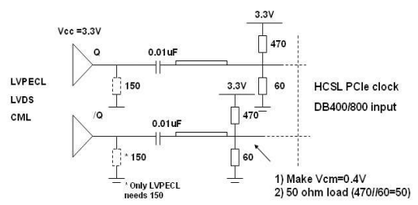


Gigabit Ethernet - ETH0

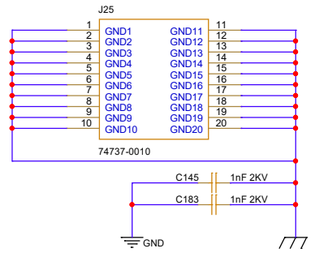


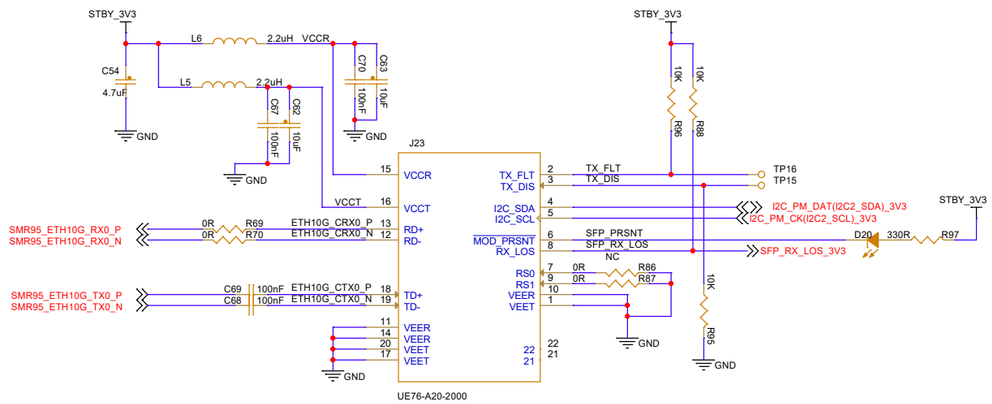
ETH 10G ref clk 156.25MHz LVDS





10G Ethernet SFP+ Copper/Fiber Only for SMR95





SFP I2C ADDRESS= 0x50 & 0x51

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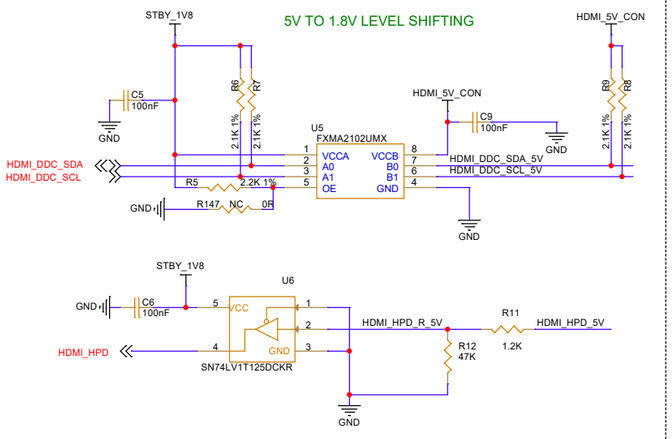
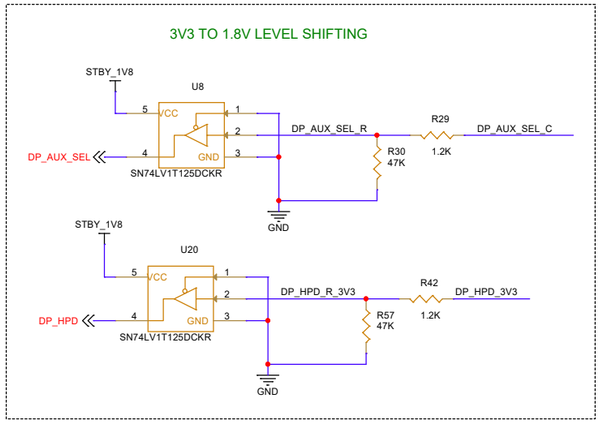
Title: 05. ETHERNET			
Size: A2	Document Number: ECHO CUSTOMBOARD	Project: ECHO-BOARD	Rev: 1.1
Designer: Shay V.		Approved By:	
Date: Wednesday, January 21, 2026		Sheet 7 of 16	

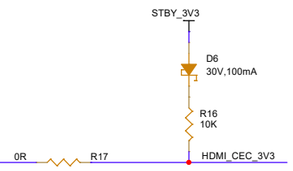
06. HDMI, DSI &DP

5V TO 1.8V LEVEL SHIFTING

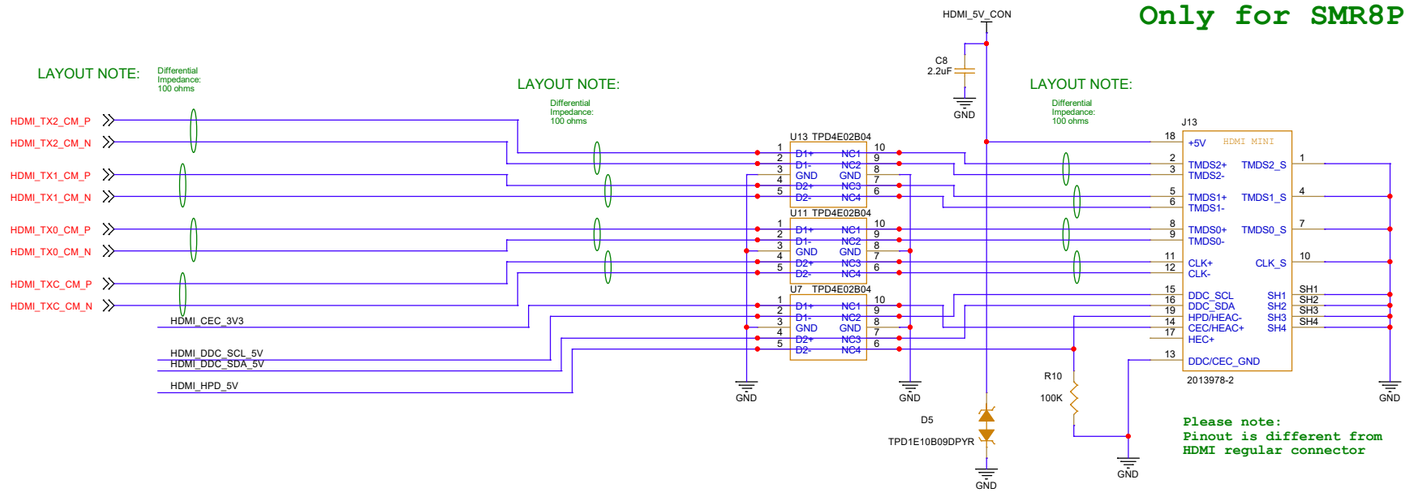


3V3 TO 1.8V LEVEL SHIFTING

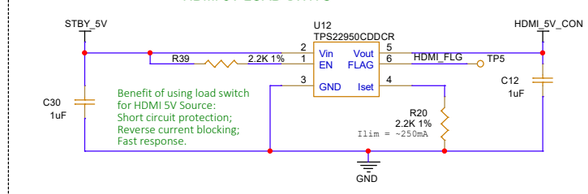




HDMI OUT MINI CONNECTOR Only for SMR8P

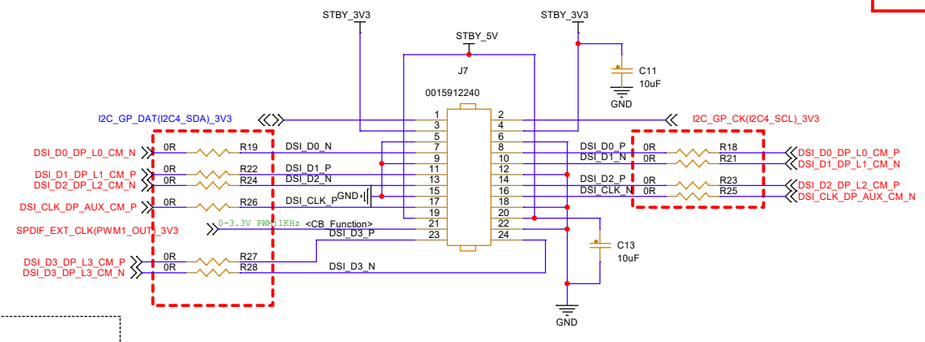


HDMI 5V LOAD SWITC

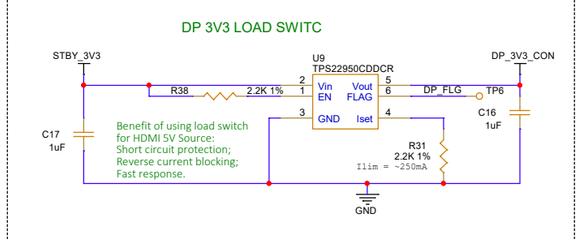


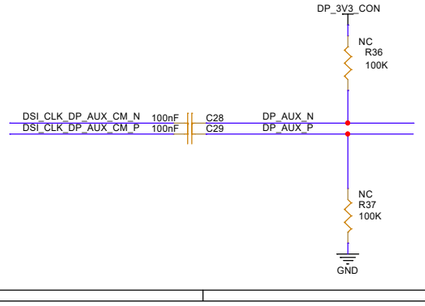
DSI DISPLAY

Note
MX8M-PLUS DSI - Assemble Res 0 ohm/0402
MX95 - Assemble Cap 100nF/0402

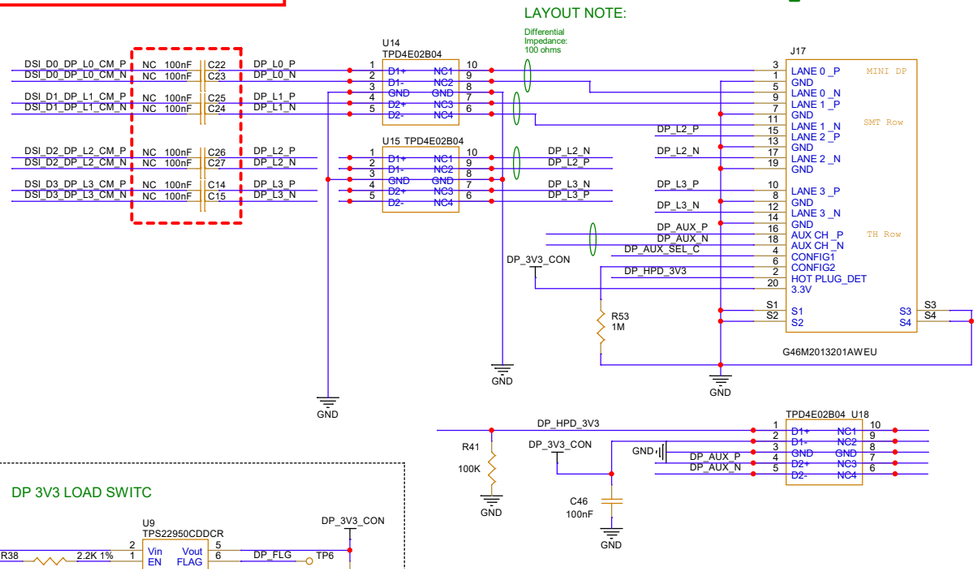


DP 3V3 LOAD SWITC





DP OUT MINI CONNECTOR Only for SMR95



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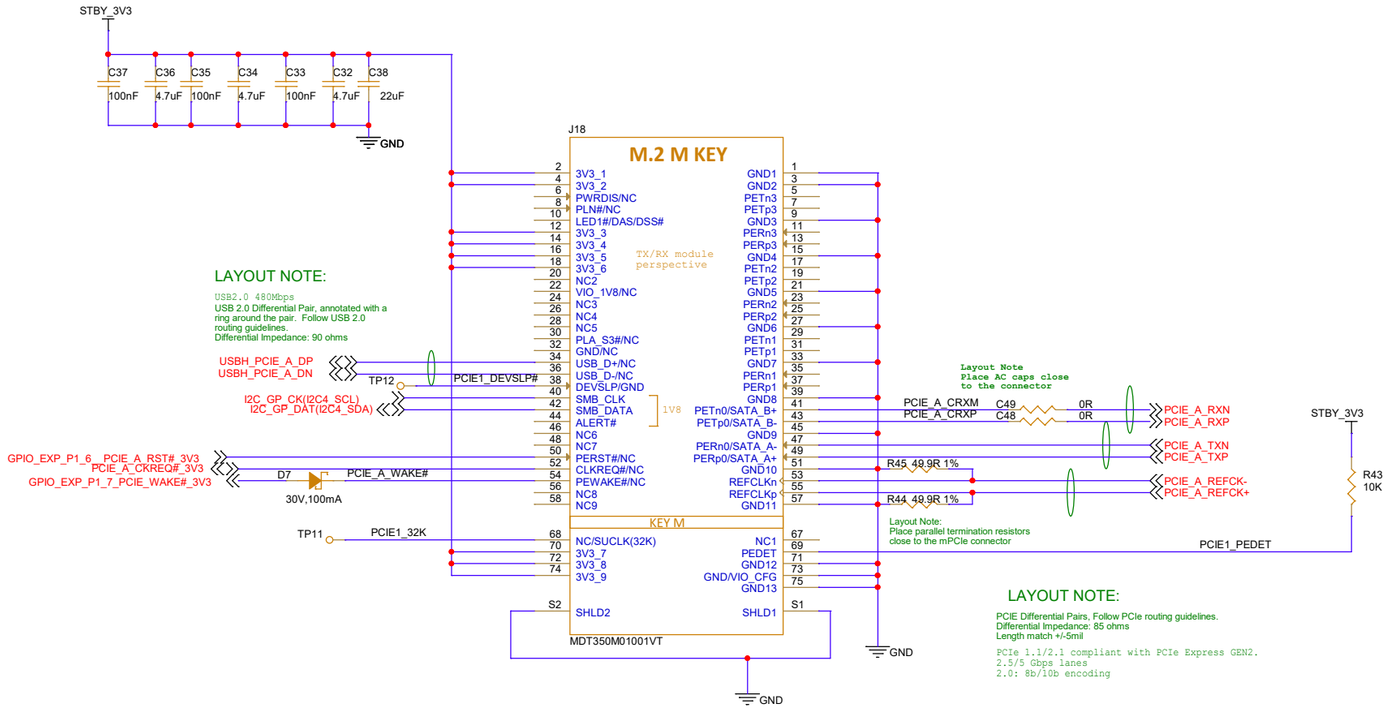
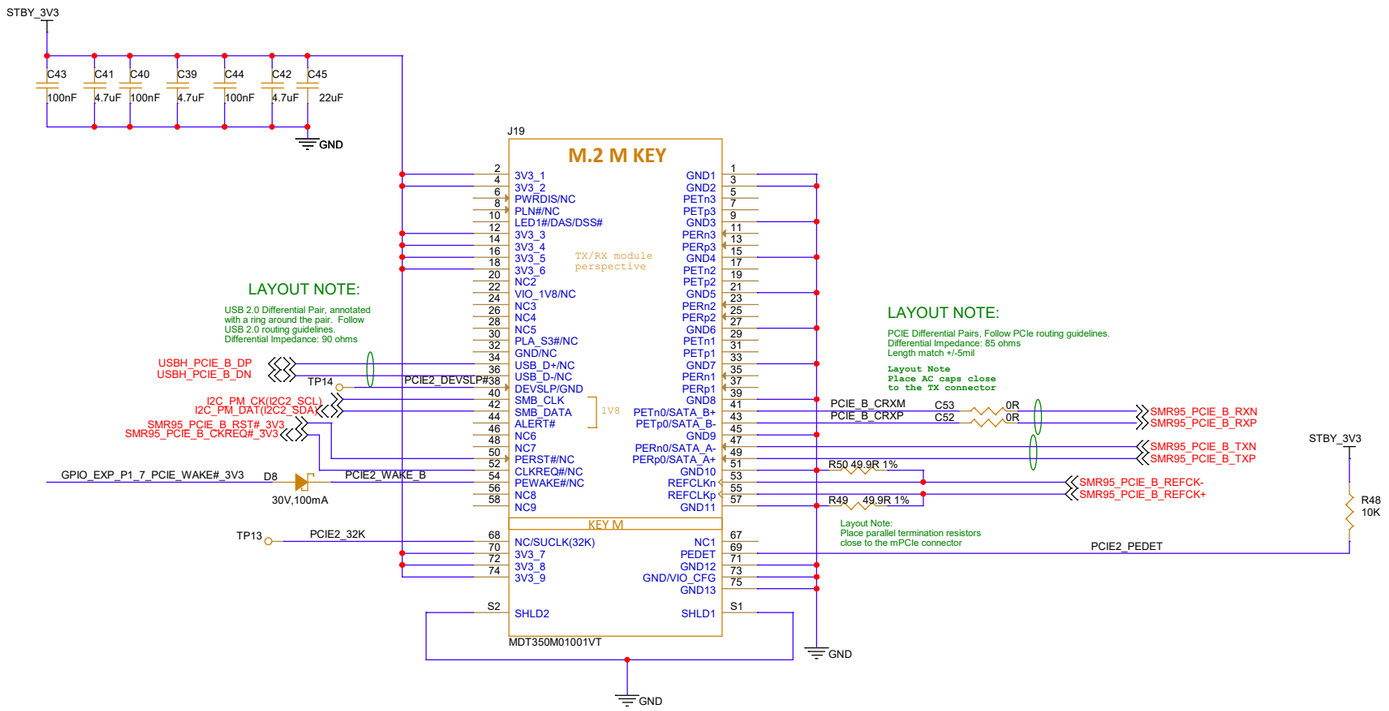
Title: 06. HDMI, DSI & DP			
Size: A2	Document Number: ECHO CUSTOMBOARD	Project: ECHO-BOARD	Rev: 1.1
Designer: Shay V.		Approved By:	<Approved By>
Date: Wednesday, February 11, 2026		Sheet 8 of 16	

07. PCIe

PCIE A M.2 M Key Vertical Connector



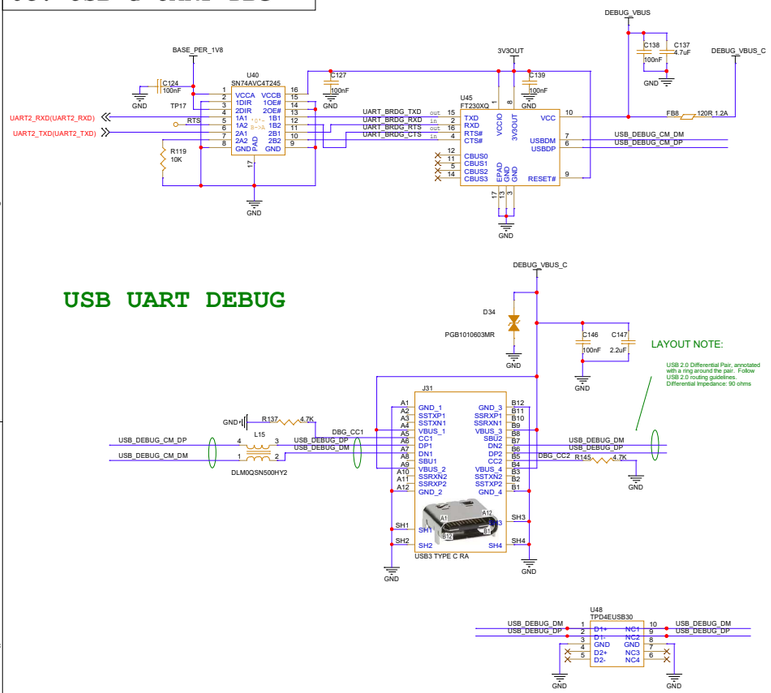
PCIE B M.2 M Key Vertical Connector
Only for SMR95



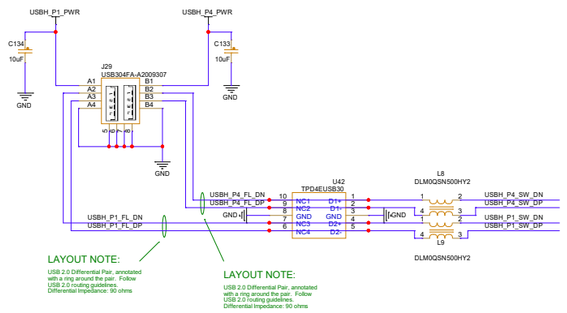
Title: 07. PCIe			
Size: C	Document Number: ECHO CUSTOMBOARD	Project: ECHO-BOARD	Rev: 1.1
Designer: Shay V.		Approved By: <Approved By>	
Date: Wednesday, January 21, 2026		Sheet 9 of 16	

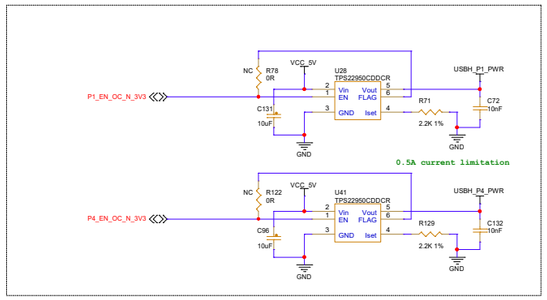
08. USB & UART DBG

USB UART DEBUG

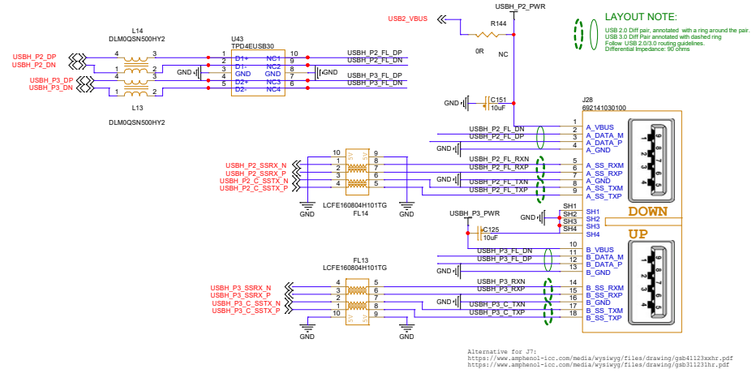


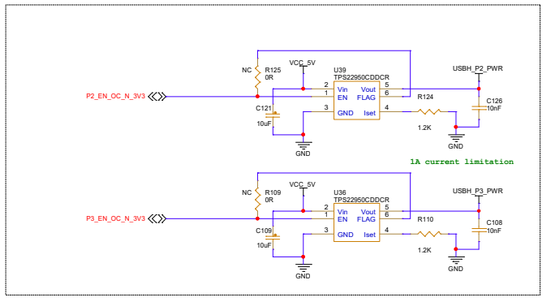
USB2.0 Type-A Dual Connector





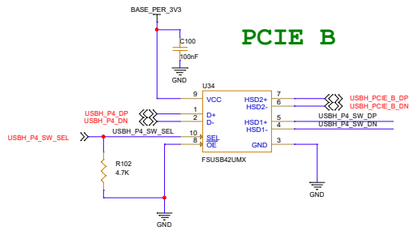
USB3.0 Type-A Dual Connector



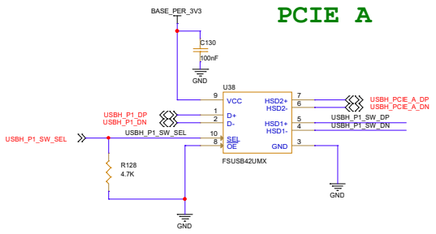


USB2.0 Switch to PCIE M.2 Connectors

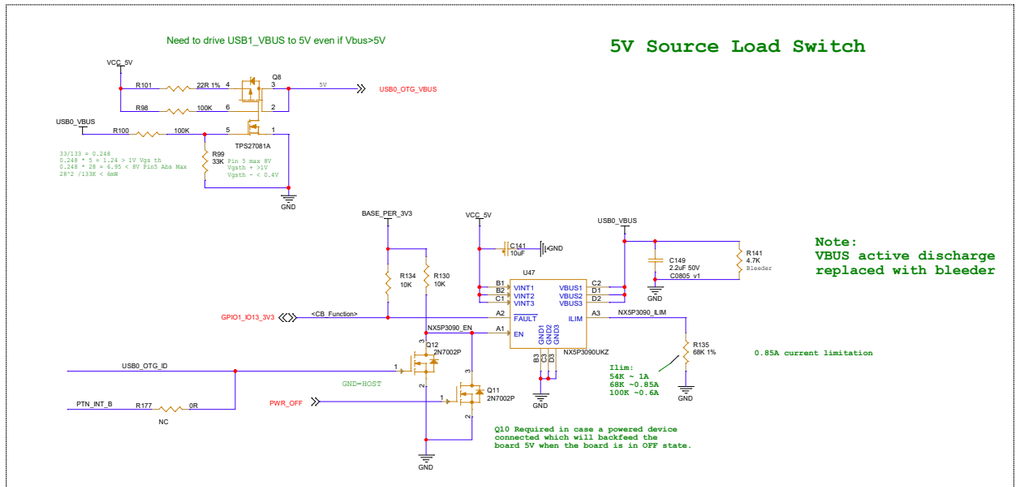
PCIE B



PCIE A

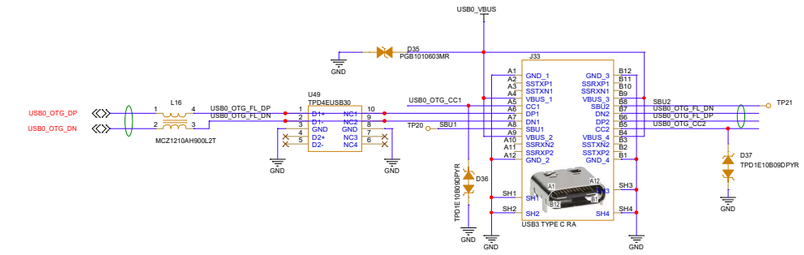


5V Source Load Switch

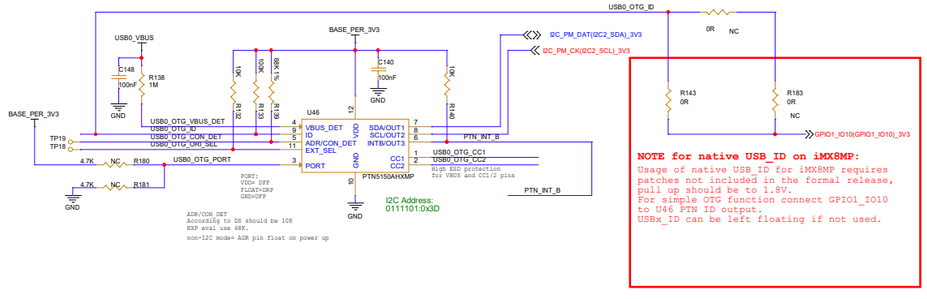


USB Type-C DRP/DRD USB 2.0 without USB PD

A DRP can dynamically switch between being a power source (like a charger) and a power sink (like a device being charged).
A DRD can switch between acting as a host (DFP) and a device (UFP) for data.
DRP/DRD USB 2.0 port without USB PD is limited to the standard USB 2.0 power delivery of 5V and up to 3A (15W).



Config Channel Logic Detection & Indication of Plug Orientation



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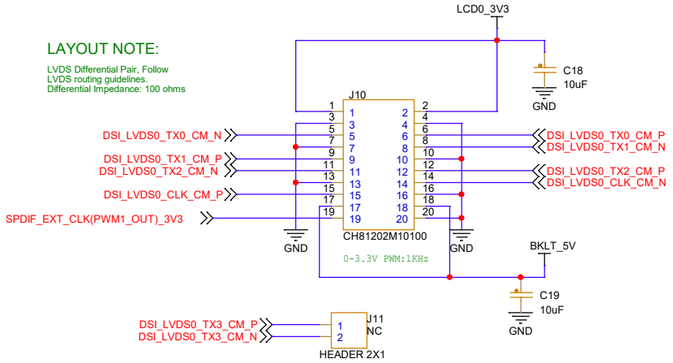
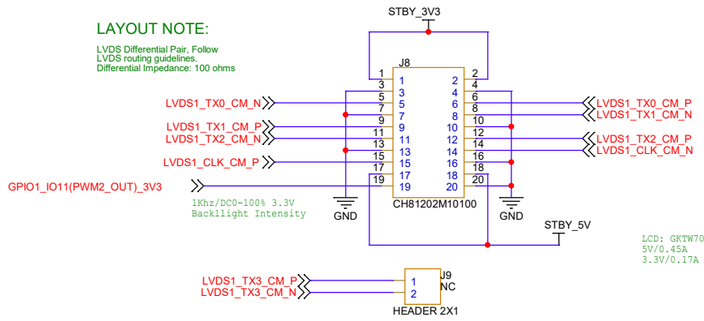
Title: 08. USB & UART DBG			
Size: A1	Document Number: ECHO CUSTOMBOARD	Project: ECHO-BOARD	Rev: 1.1
Designer: Shay V.		Approved By:	
Date: Monday, February 16, 2026		Sheet 10 of 16	

09. LCD & CSI

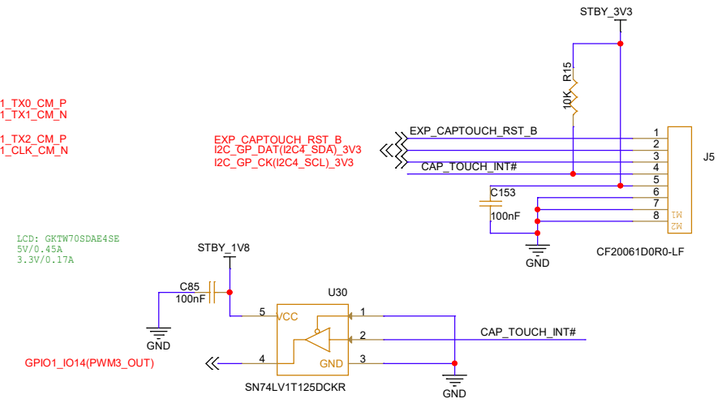
LVDS CH0/DSI Prim. Display



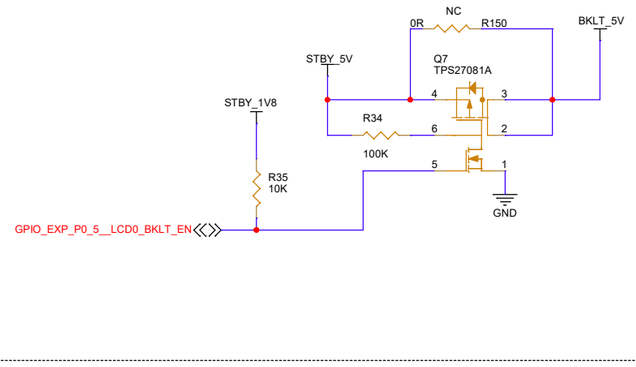
LVDS CH1 Sec. Display

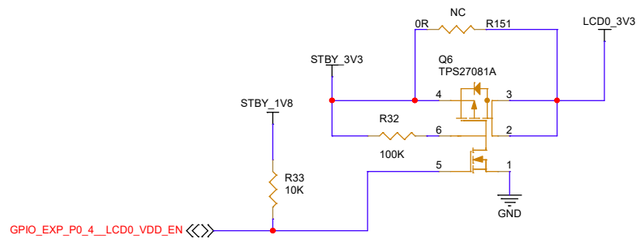


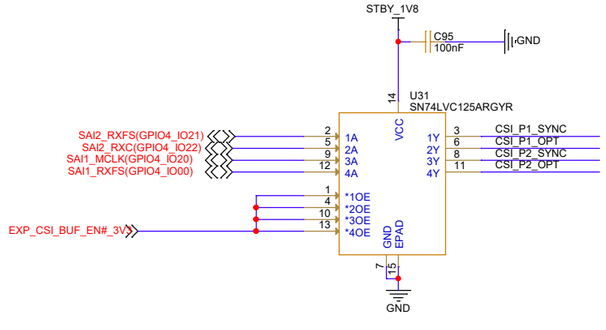
Capacitive Touch

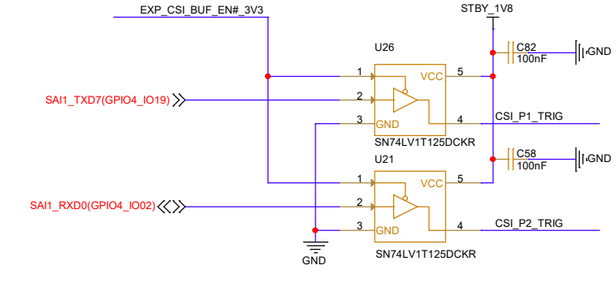


Prim. Display Ctrl





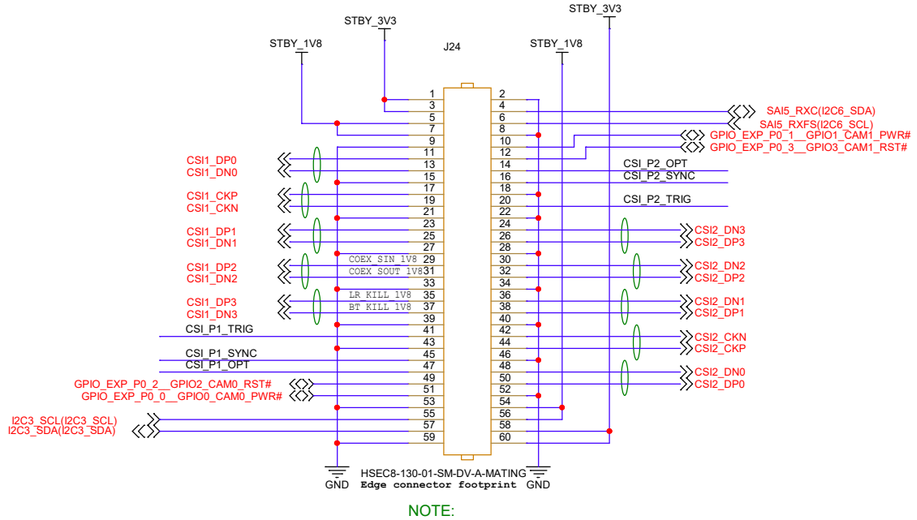




MIPI-CSI0 + MIPI-CSI1

Connects to Variscite Custom MIPI-CSI2 Camera Board
Qualified with x2 OV5640.

LAYOUT NOTE:
Differential Impedance:100 ohms
SE 50 ohms
HS mode: DIFF
LP mode: SE
Lane rate 1.5Gbps



NOTE:
1. I2C and GPIO run @ 1.8V
2. Camera reference clock generated on camera board
3. SN74AVC4T245 DIR+OE ref'd to VccA

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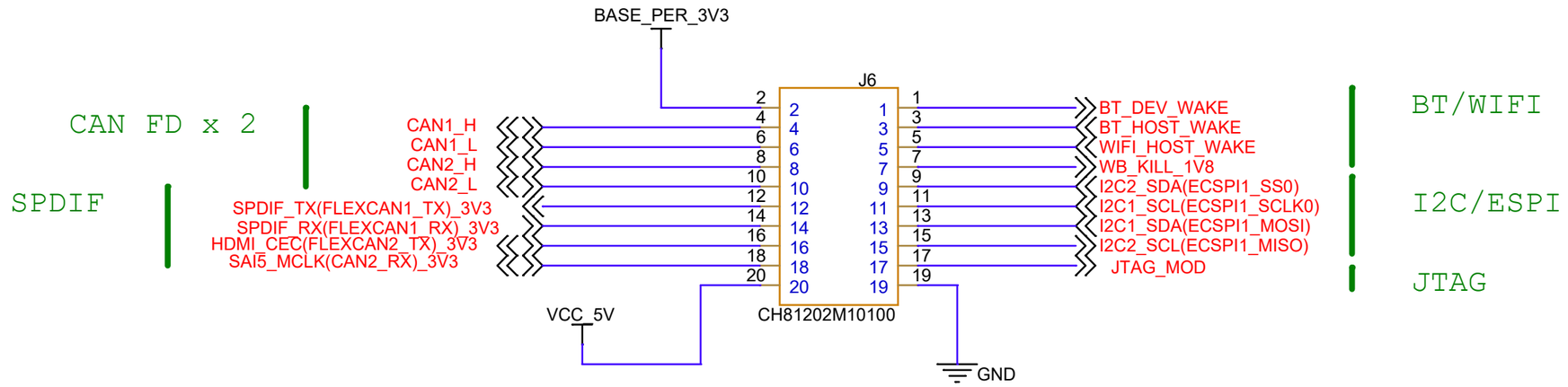
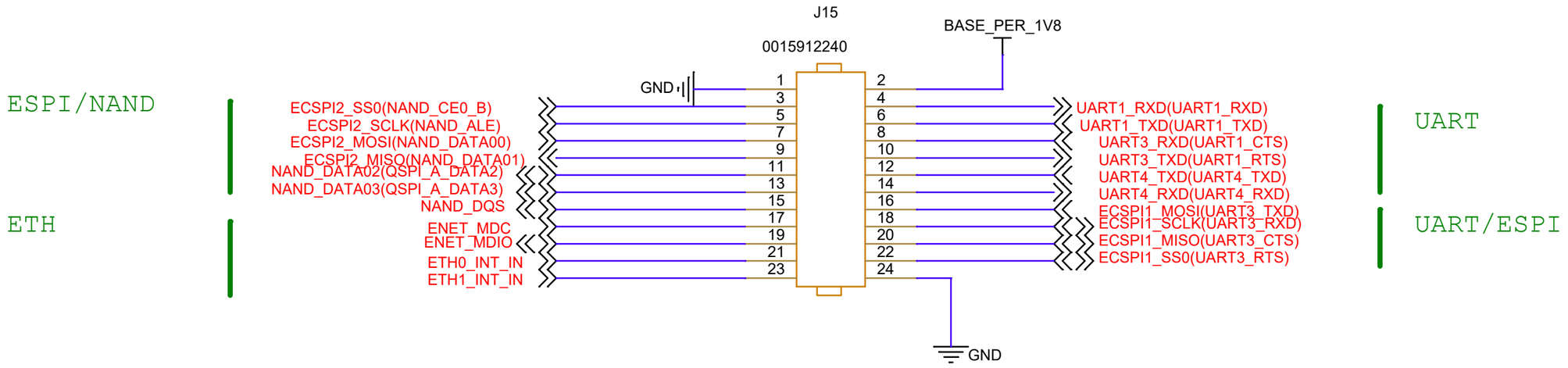
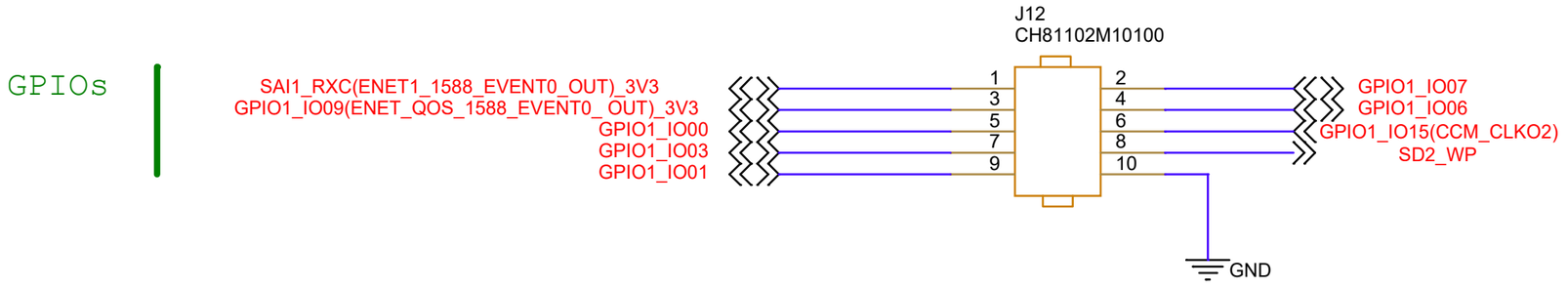
Title: 09. LCD & CSI			
Size: C	Document Number: ECHO CUSTOMBOARD	Project: ECHO-BOARD	Rev: 1.1
Designer: Shay V.		Approved By:	
Date: Sunday, February 08, 2026		Sheet 11 of 16	

10. HEADERS







variscite

Title: 10. Headers, Mechanics			
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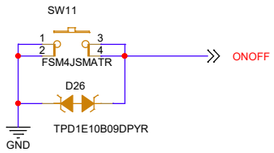
11. BOOT CONFIG & MECHANICS

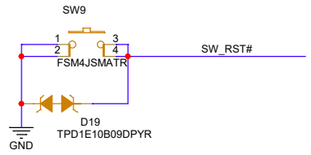
ON/OFF

PU Included on SOM



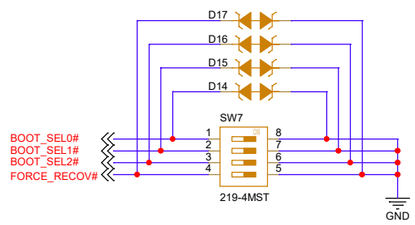
12V input - Module is in Off state
PWR SW on --> 12V is applied - Module is in RunTime mode
Press ON/OFF --> Module is in Standby mode
Press On/OFF again --> Module is in RunTime mode

RST SW



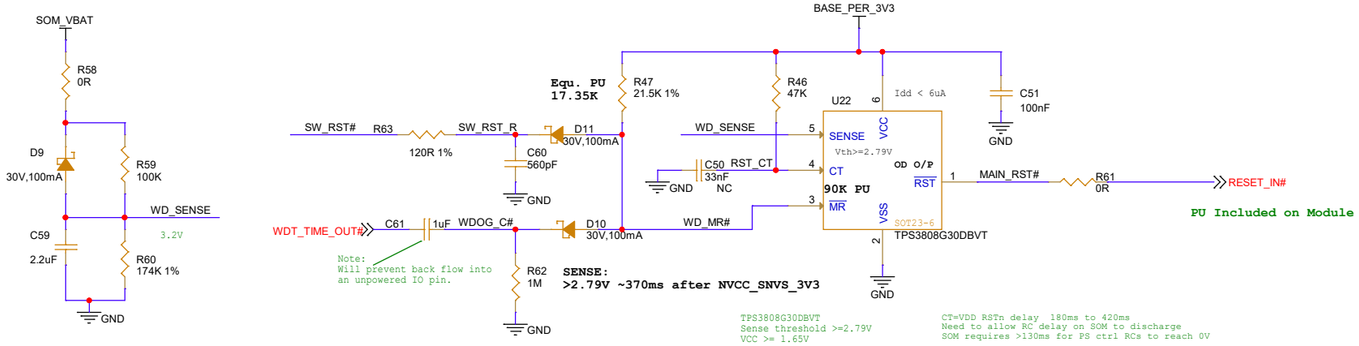
BOOT Options

PUs Included on Module



FR	BS2	BS1	BS0	
1	0	0	0	QSPI
1	0	0	1	SD
1	0	1	1	SPI
1	1	1	0	eMMC
0	X	X	X	USB Serial Download

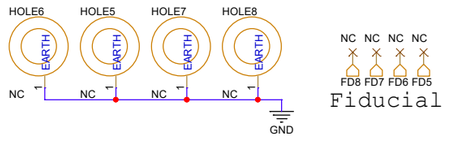
RESET & WATCHDOG



MECHANICS

SOM MOUNTING STANDOFF
Place on TOP

CHASSIS HOLES

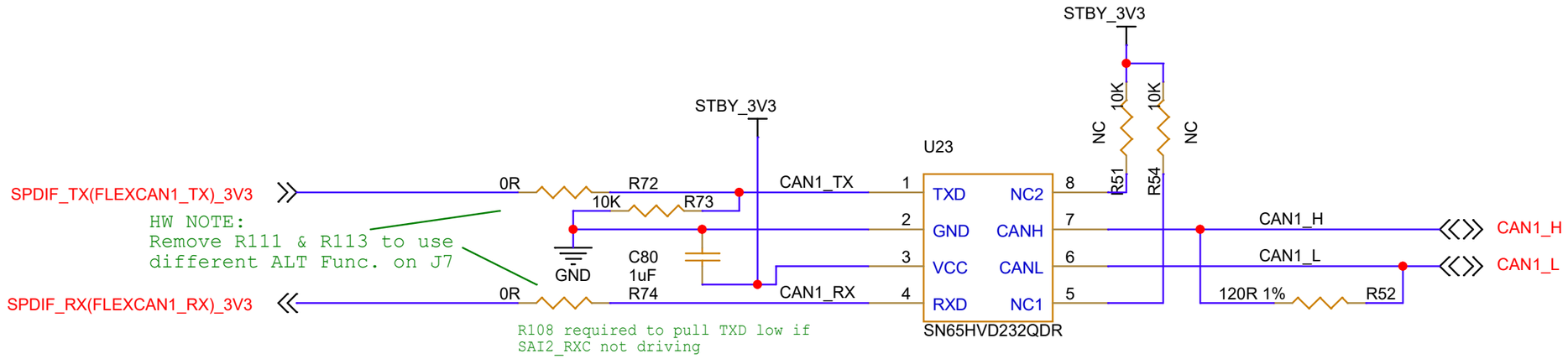


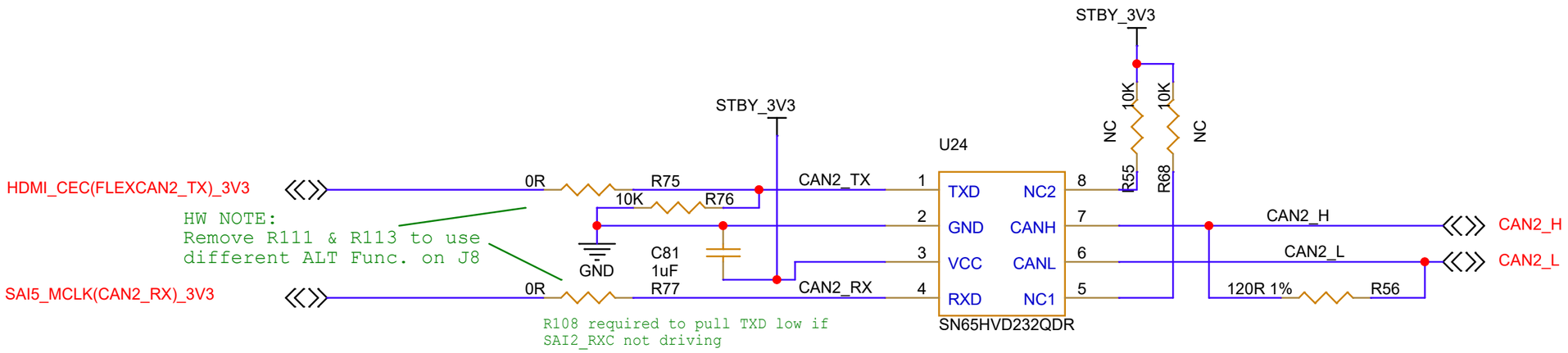
variscite

Title: 11. BOOT CONFIG & MODE			
Size: C	Document Number: ECHO CUSTOMBOARD	Project: ECHO-BOARD	Rev: 1.1
Designer: Shay V.		Approved By:	
Date: Monday, February 16, 2026		Sheet 13 of 16	

12. CAN FD INTERFACE

CAN PHY
5Mb/s Limited





variscite

Title: 12. CAN FD Interface			
Size: A4	Document Number: ECHO CUSTOMBOARD	Project: ECHO-BOARD	Rev: 1.1
Designer: Shay V.		Approved By:	
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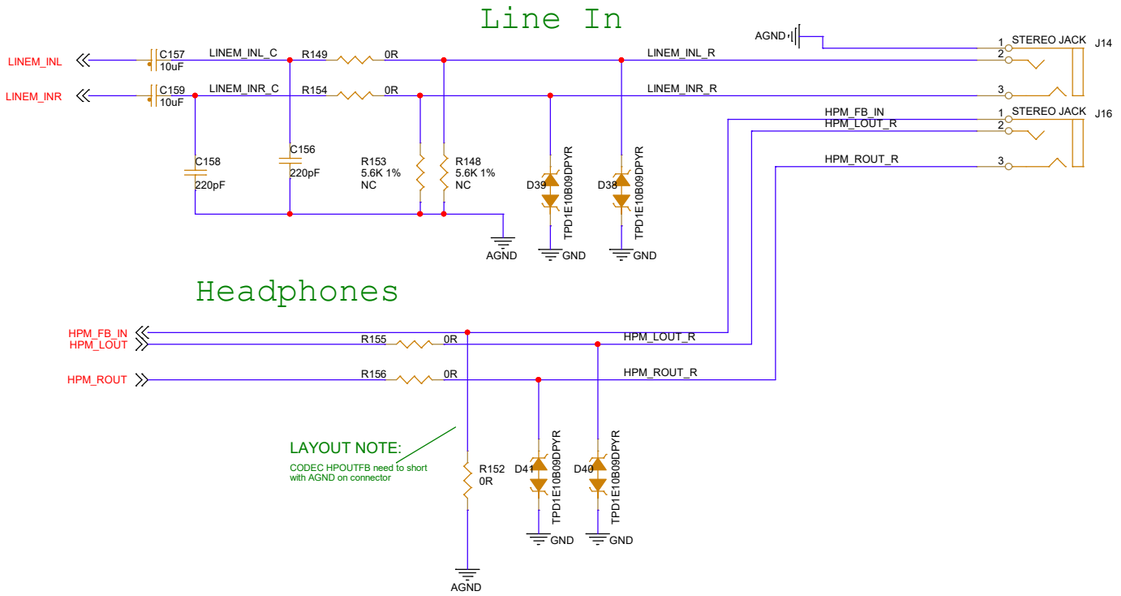
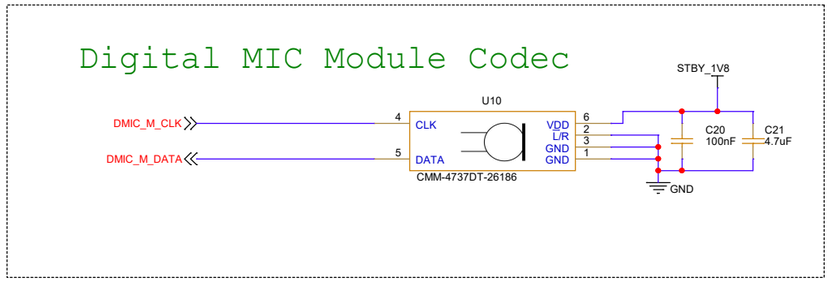
13. AUDIO

Audio Analog Module Codec



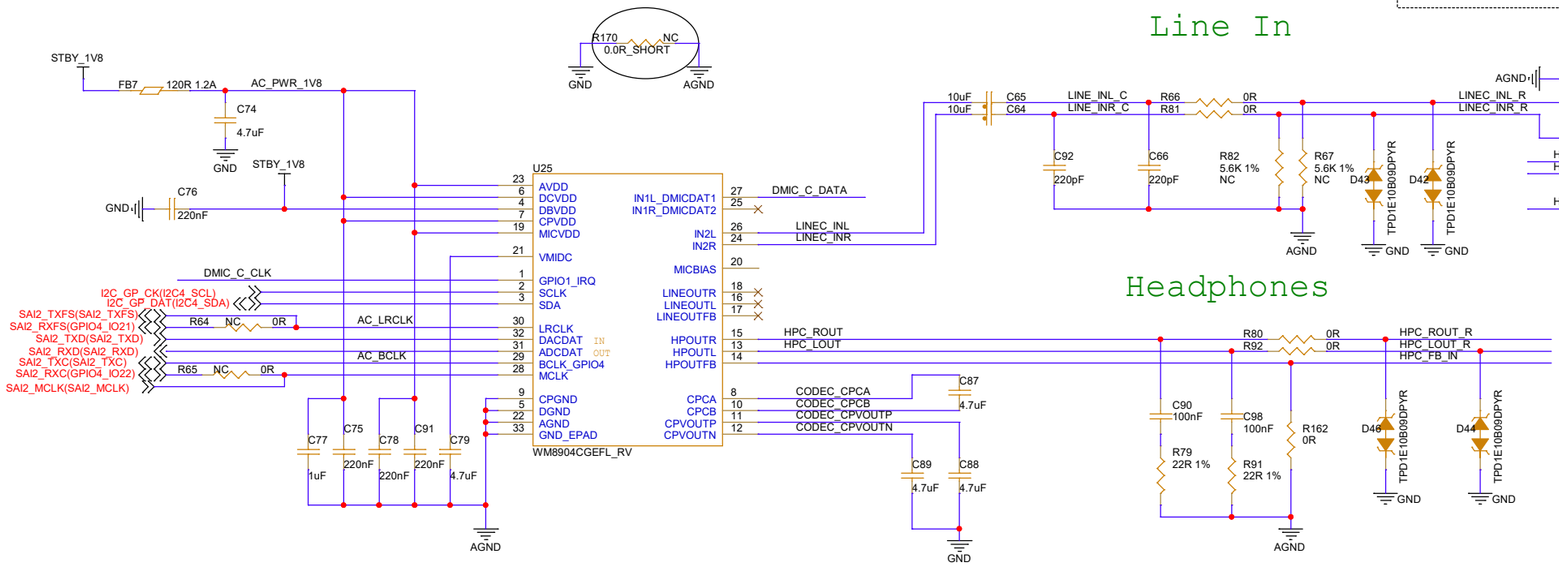
Line In
Upper Jack

Headphones
Lower Jack

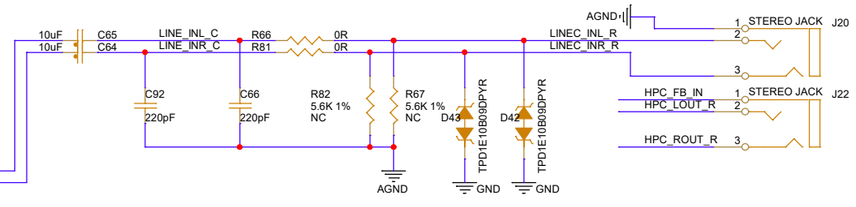


Audio Analog Carrier Codec

DBVDD- SMARC changed from 3.3V-> 1.8V



Line In



Line In
Upper Jack

Headphones
Lower Jack

Headphones

Title: 13. Audio			
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Designer: Shay V.		Approved By:	
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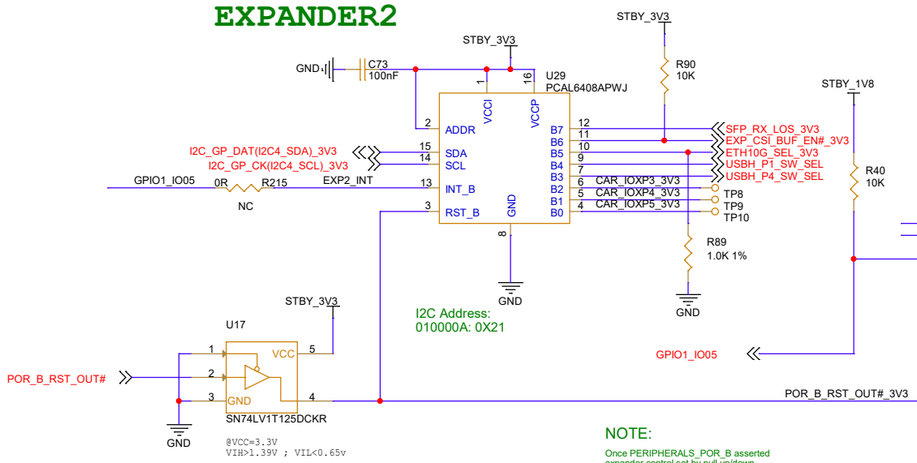
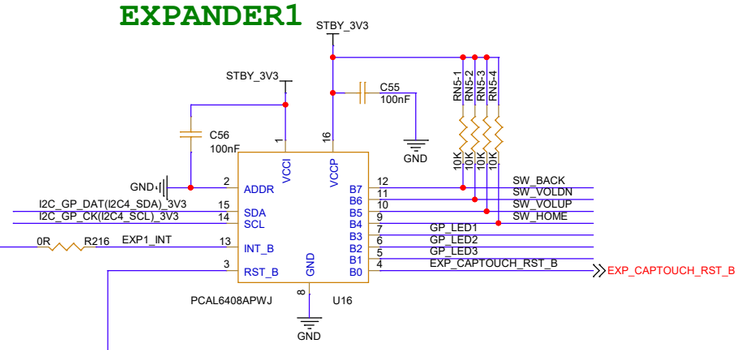
14. GPIO

GPIO EXPANDER2



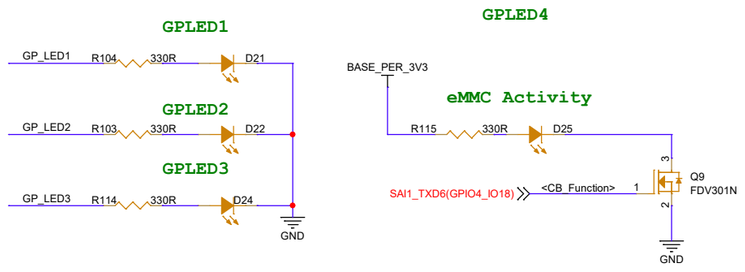
GPIO EXPANDER1



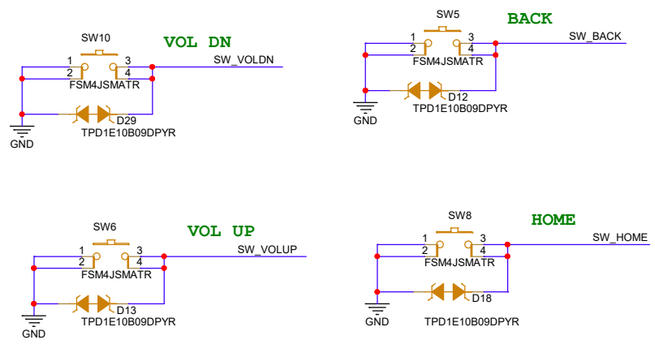
NOTE:

Once PERIPHERALS_POR_B asserted expander control set by pull up/down.

GP LEDS



GP BUTTONS



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Title: 14. GPIO			
Size: C	Document Number: ECHO CUSTOMBOARD	Project: ECHO-BOARD	Rev: 1.1
Designer: Shay V.		Approved By:	
Date: Wednesday, January 21, 2026		Sheet 16 of 16	