Rev. 1.0, 3/2026

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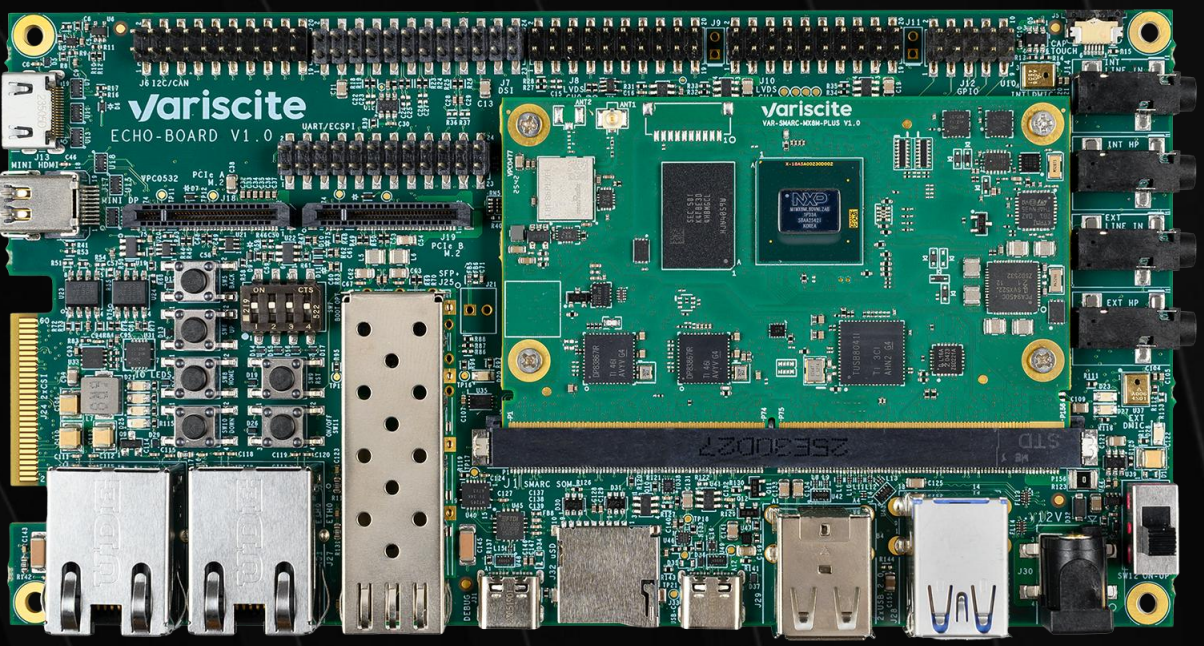
VARISCITE LTD.

ECHO-BOARD V1.1 Datasheet
Carrier-board for:
VAR-SMARC-MX8M-PLUS



VARISCITE LTD.

Echo-Board Datasheet

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1. Revision History

Revision	Date	Notes
1.0	March 03, 2026	Initial - Preliminary

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4. Overview

This chapter provides an overview of the ECHO-Board.

4.1 General Information

ECHO-Board is a complete development board, utilizing all of the VAR-SMARC-MX8M-PLUS System-on-Modules features. It is assembled with large variety of user and debug interfaces enabling it to serve as both a complete development kit or a stand-alone end-product.

Supported Variscite products:

- VAR-SMARC-MX8M-PLUS
- TBD

Contact Variscite support services for further information: support@variscite.com.

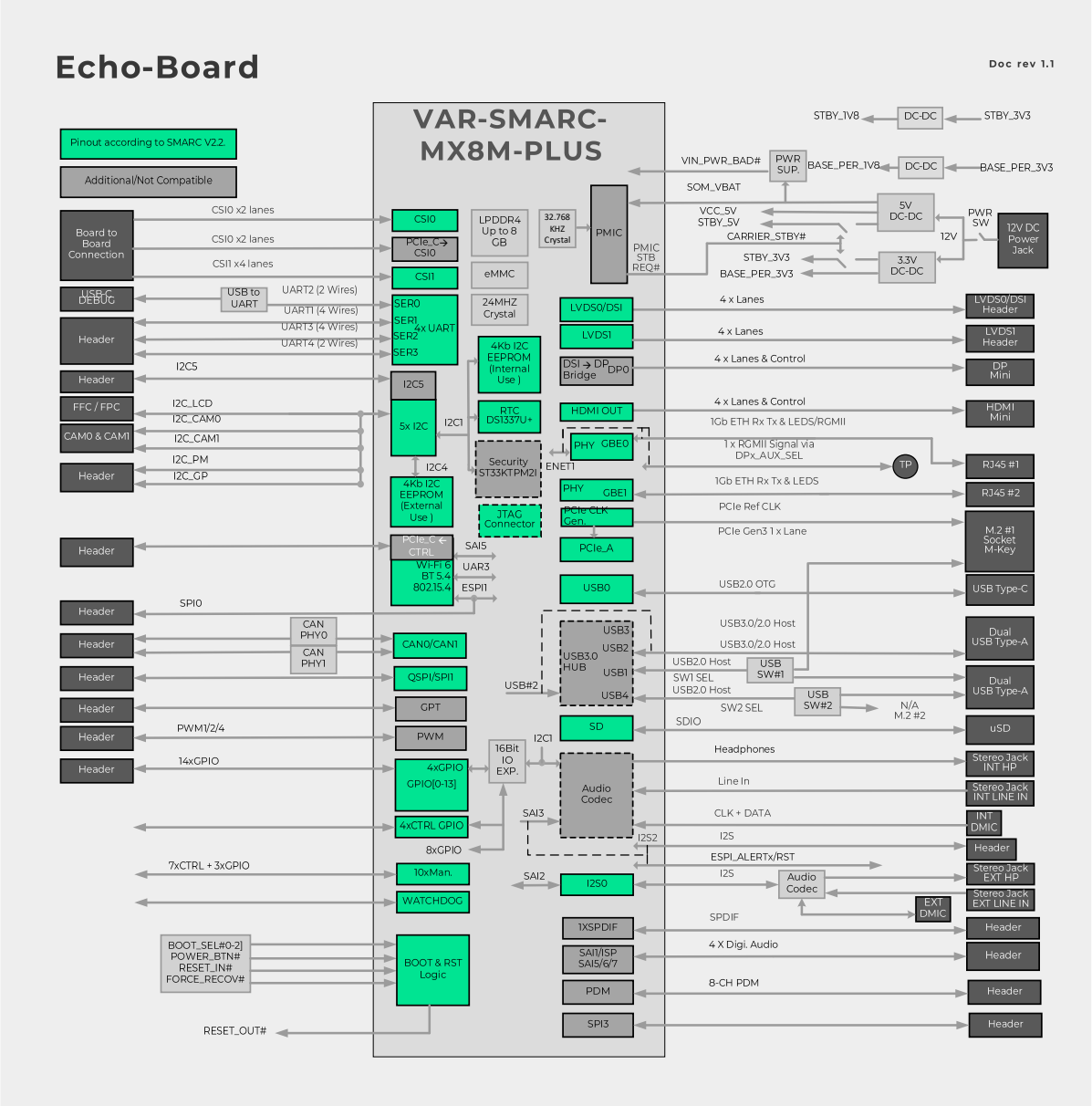
5. Feature Summary

- SMARC revision 2.2 compliant
- Display
  - 2 x 18 bit LVDS Interface supporting Variscite's 7" TFT capacitive touch LCD
  - HDMI 2.0a via mini-HDMI connector
  - DSI
- Touch panel interface
  - Capacitive - I2C based
- Ethernet
  - 2 x 10/100/1000BaseT – RJ45
- PCIe
  - M.2 M-Key PCIe interfaces
- USB
  - 1 x USB2.0 OTG Type-C
  - 2 x USB3.0 Host Type-A
  - 2 x USB2.0 Host Type-A
- Audio two interfaces:
  - Internal – CODEC on SOM
    - 3.5mm Headphones jack
    - 3.5mm Line in jack
    - Digital Microphone
  - External – CODEC on Carrier
    - 3.5mm Headphones jack
    - 3.5mm Line in jack
    - Digital Microphone
- µSD-Card slot
- Camera
  - 1 x MIPI CSI 4 - lanes
  - 1 x MIPI CSI 2 - lanes

- Debug
  - USB debug (UART2) – USB Type-C
- Additional Interfaces
  - SAI (Serial Audio Interfaces) – Headers
  - UART, QSPI, ECSPI, I2C, GPIO's – Headers
  - CAN Bus 5Mb/s CAN PHY – Header
  - General purpose LEDs, Buttons
- Power
  - 12V DC input – 2.0mm DC jack / 2 pins Terminal Block
  - 5V/12V DC Out – 2 pin Header FAN Power
  - 12V LDO for RTC backup
  - RTC Backup battery (Not Assembled) - CR1225 Battery Holder

5.1 Block Diagram

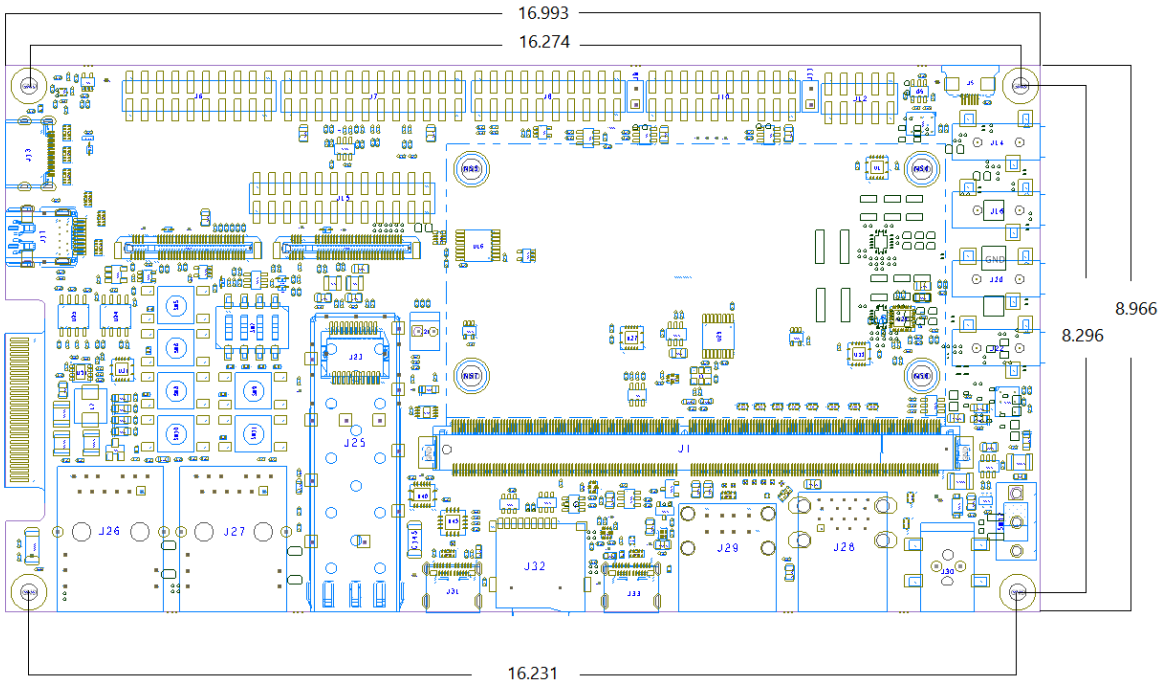
Figure 1 ECHO-BOARD Block Diagram



5.2 Board Layout

The ECHO-BOARD physical dimensions are 169.9 x 89.6 mm.

Figure 2 ECHO-BOARD Physical Dimensions



Detailed CAD files are available for download at www.variscite.com.

5.3 ECHO-BOARD Connectors

The below table lists all available connectors on ECHO-BOARD,
Refer to chapter 2 for a more detailed description and Pin-out of each connector.

Table 5-1 ECHO-BOARD connectors

Reference	Function	Type
J1	MXM-3 SMARC connector	Board to board, 314 pos., 0.5mm
J5	Capacitive Touch Panel I/F	FFC/FPC 6-pin
J6	CAN Bus, SPDIF, I2C, WIFI/BT IOs	Header SMT, 10x2, 2.54mm
J7	DSI	Header SMT, 12x2, 2.54mm
J8	LVDS#1 (Clock & Data pairs 0-2)	Header SMT, 10x2, 2.54mm
J9	LVDS#1 (Data pair 3)	Header TH, 2x1, 2.54mm
J10	LVDS#0/DSI (Clock & Data pairs 0-2)	Header SMT, 10x2, 2.54mm
J11	LVDS#0/DSI (Data pair 3)	Header TH, 2x1, 2.54mm
J12	GPIOs	Header SMT, 5x2, 2.54mm
J13	HDMI	HDMI Type C (mini) Rcpt. SMT, R/A
J14	Line In external CODEC	Audio Jack 3.5 mm
J15	UART, ESPI, NAND	Header SMT, 12x2, 2.54mm
J16	Headphones external CODEC	Audio Jack 3.5 mm
J17	Display Port - future use	Mini DP Rcpt. R/A
J18	PCIe A	M.2 M-KEY, Vertical Connector
J19	PCIe B – future use	M.2 M-KEY, Vertical Connector
J20	Line In internal CODEC	Audio Jack 3.5 mm
J21	Fan 12V/5V	Header TH, 2x1, 2.54mm
J22	Headphones internal CODEC	Audio Jack 3.5 mm
J23	10Gb ETH Port	SFP+ Receptacle SMT, 2x10
J24	MIPI-CSI (4 lanes x 2 Cameras)	Edge Connector mates to HSEC8-130-01-SM-DV-A
J25	10Gb ETH Port	SFP+ Cage TH Connector
J26	10/100/1000Mbps ETH1 Port	RJ-45
J27	10/100/1000Mbps ETH0 Port	RJ-45
J28	USB 3.0 Host x2	USB 3.0 Type A Stacked
J29	USB 2.0 Host x2	USB 2.0 Type A Stacked
J30	12V Power in	DC In Jack 2.0 mm
J31	USB Debug	USB Type C
J32	SD-MMC	uSD Connector
J33	USB 2.0 OTG	USB Type C
J34	Power In	2 Pin Terminal Block – optional
JBT5	RTC Battery Holder	CR1225 Battery Holder - optional

6. Detailed Description

6.1 Overview

This chapter details the features and external interfaces, some of which are driven directly by the following SOMs:

- VAR-SMARC-MX8M-PLUS
- TBD

Please refer to the applicable SMARC data sheet for more information.

Table 6-1 describes this chapter table headers and acronyms used.

Table 6-1: Acronyms used on tables column header

Heading	Options	Meaning
Pin#	x	**Pin number on a connector**
Type		**Pin type & direction**
	I	INPUT
	O	OUTPUT
	DS	Differential Signal
	A	Analog
	P	Power
Signal		**ECHO-BOARD schematic signal name**
Description		**Short Pin functionality description**

6.2 Functionality of ECHO-BOARD Connectors

Various products can use the same connector pins to expose different interfaces, resulting in incompatibility or loss of intended functionality.

The reason is that not all products are compatible with the same set of interfaces.
We are making every effort to make as many interfaces available on each SOC as possible and utilize any available free pins to do so.

Please refer to the specific SOM datasheet for exact pin information.

6.3 ECHO-BOARD Interfaces

6.3.1 SOM

The ECHO-BOARD features MXM-3 SMARC mating connectors that allows it to connect with all the pin-compatible SOMs listed above.
Please refer to the applicable SOM module data sheet for a complete signal description and pin-out on J1 connector.

6.4 Standard External Interfaces

6.4.1 USB HOST & OTG

SOMs USB capability is as follows:

- VAR-SMARC-MX8M-PLUS features:
  - 1 x USB2.0 OTG port – Type-C connector
  - 2 x USB2.0 Host ports – Dual Type-A connector
  - 2 x USB3.0 Host ports – Dual Type-A connector
- TBD

6.4.1.1 USB2.0 Type-C OTG Connector Pin-out (J33)

Table 6-2 USB Type-C OTG Connector Pin-out (J33)

Pin #	ECHO-BOARD Signal	Type	Description
A1	GND	P	Ground return
A2			
A3			
A4	USB0_VBUS	P	Port0 Bus power
A5	USB0_OTG_CC1	IO	Port0 Configuration channel
A6	USB0_OTG_FL_DP	DSIO	Port0 Non-SuperSpeed diff. pair, pos. 1, positive
A7	USB0_OTG_FL_DN	DSIO	Port0 Non-SuperSpeed diff. pair, pos. 1, negative
A8	SBU1	IO	Port0 Sideband use (SBU)
A9	USB0_VBUS	P	Port0 Bus power
A10			
A11			
A12	GND	P	Digital Ground
B1	GND	P	Digital Ground
B2			
B3			
B4	USB0_VBUS	P	Port0 Bus power
B5	USB0_OTG_CC2	IO	Port0 Configuration channel
B6	USB0_OTG_FL_DP	DSIO	Port0 Non-SuperSpeed diff. pair, pos. 2, positive

Pin #	ECHO-BOARD Signal	Type	Description
B7	USB0_OTG_FL_DN	DSIO	Port0 Non-SuperSpeed diff. pair, pos. 2, negative
B8	SBU2	IO	Port0 Sideband use (SBU)
B9	USB0_VBUS	P	Port0 Bus power
B10			
B11			
B12	GND	P	Digital Ground
SH1	GND	P	SHIELD pin reference
SH2	GND	P	SHIELD pin reference
SH3	GND	P	SHIELD pin reference
SH4	GND	P	SHIELD pin reference

6.4.1.2 Dual USB3.0 HOST Connector Pin-out (J28)

Table 6-3 Dual USB3.0 Host Connector Pin-out (J28)

Pin #	ECHO-BOARD Signal	Type	Description
1	USBH_P2_PWR	P	Port2 Bus power
2	USBH_P2_FL_DN	DSIO	Port2 Non-SuperSpeed diff. pair, negative
3	USBH_P2_FL_DP	DSIO	Port2 Non-SuperSpeed diff. pair, positive
4	GND	P	Digital Ground
5	USBH_P2_FL_RXN	DSI	Port2 SuperSpeed diff. pair RX, negative
6	USBH_P2_FL_RXP	DSI	Port2 SuperSpeed diff. pair RX, positive
7	GND	P	Digital Ground
8	USBH_P2_FL_TXN	DSO	Port2 SuperSpeed diff. pair TX, negative
9	USBH_P2_FL_TXP	DSO	Port2 SuperSpeed diff. pair TX, positive
10	USBH_P3_PWR	P	Port 3 Bus power
11	USBH_P3_FL_DN	DSIO	Port3 Non-SuperSpeed diff. pair, negative
12	USBH_P3_FL_DP	DSIO	Port3 Non-SuperSpeed diff. pair, positive
13	GND	P	Digital Ground
14	USBH_P3_RXN	DSI	Port3 SuperSpeed diff. pair RX, negative
15	USBH_P3_RXP	DSI	Port3 SuperSpeed diff. pair RX, positive
16	GND	P	Digital Ground
17	USBH_P3_C_TXN	DSO	Port3 SuperSpeed diff. pair TX, negative
18	USBH_P3_C_TXP	DSO	Port3 SuperSpeed diff. pair TX, positive
SH1	GND	P	SHIELD pin reference
SH2	GND	P	SHIELD pin reference
SH3	GND	P	SHIELD pin reference
SH4	GND	P	SHIELD pin reference

6.4.1.3 Dual USB2.0 HOST Connector Pin-out (J29)

Table 6-4 Dual USB2.0 Host Connector Pin-out (J29)

Pin #	ECHO-BOARD Signal	Type	Description
A1	USBH_P1_PWR	P	Port1 Bus power
A2	USBH_P1_FL_DN	DSIO	Port1 Non-SuperSpeed diff. pair, negative
A3	USBH_P1_FL_DP	DSIO	Port1 Non-SuperSpeed diff. pair, positive
A4	GND	P	Digital Ground
B1	USBH_P4_PWR	DSI	Port4 Bus power
B2	USBH_P4_FL_DN	DSI	Port4 Non-SuperSpeed diff. pair, negative
B3	USBH_P4_FL_DP	DSO	Port4 Non-SuperSpeed diff. pair, positive
B4	GND	P	Digital Ground
SH1	GND	P	SHIELD pin reference
SH2	GND	P	SHIELD pin reference
SH3	GND	P	SHIELD pin reference
SH4	GND	P	SHIELD pin reference

Note:

It is important to be aware that USB ports 1 & 4 signals are multiplexed with M.2 PCIe interfaces. Default interface is set to support USB. Mux select signals are connected to I/O Expander #2, please refer to ECHO-BOARD schematics.

6.4.2 uSD Card interface is driven by SD/MMC2 interface

Table 6-5 uSD Card Slot Connector Pin-out (J32)

Pin #	ECHO-BOARD Signal	Type	Description
1	SD2_DATA2	IO	MMC Parallel Data2
2	SD2_DATA3	IO	MMC Parallel Data3
3	SD2_CMD	IO	MMC Command
4	SW_3P3_SD2	P	3.3V supply
5	SD2_CLK_R	I	MMC Clock
6	GND	P	Digital Ground
7	SD2_DATA0	IO	MMC Parallel Data0
8	SD2_DATA1	IO	MMC Parallel Data1
9	SD2_CD_B(SD2_CD_B)	O	MMC Card Detect
10	GND	P	SHIELD pin reference
11	GND	P	SHIELD pin reference
12	GND	P	SHIELD pin reference
13	GND	P	SHIELD pin reference

6.4.3 M.2 PCIe Slots

The ECHO-BOARD exports two PCIe ports through standard M.2 M-Key slots, supporting variety of M.2 cards.

6.4.3.1 M.2 PCIe A Connectors Pin-out (J18 & J19)

SOMs PCIe capabilities is as follows:

- VAR-SMARC-MX8M-PLUS has one PCIe interface – J18 only
- TBD has two PCIe interfaces – J18 & J19

Table 6-6 PCIe A Connector Pinout (J18)

Pin #	ECHO-BOARD Signal	Type	Description
1	GND	P	Digital Ground
2	STBY_3V3	P	Stand by 3.3V
3	GND	P	Digital Ground
4	STBY_3V3	P	Stand by 3.3V
5			
6			
7			
8			
9	GND	P	Digital Ground
10			
11			
12	STBY_3V3	P	Stand by 3.3V

Pin #	ECHO-BOARD Signal	Type	Description
13			
14	STBY_3V3	P	Stand by 3.3V
15	GND	P	Digital Ground
16	STBY_3V3	P	Stand by 3.3V
17			
18	STBY_3V3	P	Stand by 3.3V
19			
20			
21	GND	P	Digital Ground
22			
23			
24			
25			
26			
27	GND	P	Digital Ground
28			
29			
30			
31			
32			
33	GND	P	Digital Ground
34	USBH_PCIE_A_DP	DSIO	USB2.0 Diff. Positive; Multiplexed with USBH_P1 interface
35			
36	USBH_PCIE_A_DN	DSIO	USB2.0 Diff. Negative; Multiplexed with USBH_P1 interface
37			
38	PCIE1_DEVSLP#	I	Device Sleep. Connected to Test Point
39	GND	P	Digital Ground
40	I2C_GP_CK(I2C4_SCL)	I	I2C #4 Clock, 1V8 I/O
41	PCIE_A_RXN	DSO	PCIe Transmit Lane Diff. Negative
42	I2C_GP_DAT(I2C4_SDA)	IO	I2C #4 Data, 1V8 I/O
43	PCIE_A_RXP	DSO	PCIe Transmit Lane Diff. Positive
44			
45	GND	P	Digital Ground
46			
47	PCIE_A_TXN	DSI	PCIe Receive Lane Diff. Negative
48			
49	PCIE_A_TXP	DSI	PCIe Receive Lane Diff. Positive
50	GPIO_EXP_P1_6__PCIE_A_RST#_3V3	I	PCIe Port n Reset signal.
51	GND	P	Digital Ground
52	PCIE_A_CKREQ#_3V3	O	M.2 Clock request. Connected to PCIe reference clock generator.
53	PCIE_A_REFCK-	DSI	PCIe Clock Diff. Negative; 100MHz HCSL, generated from SOM
54	PCIE_A_WAKE#	O	PCIe wake signal
55	PCIE_A_REFCK+	DSI	PCIe Clock Diff. Positive; 100MHz HCSL, generated from SOM
56			
57	GND	P	Digital Ground

Pin #	ECHO-BOARD Signal	Type	Description
58			
59-66 M-Key			
67			
68	PCIE1_32K	I	32.768 kHz clock supply input. Connected to Test Point
69	PCIE1_PEDET	I	STBY_3V3 PU
70	STBY_3V3	P	Stand by 3.3V
71	GND	P	Digital Ground
72	STBY_3V3	P	Stand by 3.3V
73	GND	P	Digital Ground
74	STBY_3V3	P	Stand by 3.3V
75	GND	P	Digital Ground
S1	GND	P	Digital Ground
S2	GND	P	Digital Ground

6.4.3.2 M.2 PCIe B Connector Pin-out (J19)

Table 6-7 PCIe B Connector Pinout (J19)

Pin #	ECHO-BOARD Signal	Type	Description
1	GND	P	Digital Ground
2	STBY_3V3	P	Stand by 3.3V
3	GND	P	Digital Ground
4	STBY_3V3	P	Stand by 3.3V
5			
6			
7			
8			
9	GND	P	Digital Ground
10			
11			
12	STBY_3V3	P	Stand by 3.3V
13			
14	STBY_3V3		Stand by 3.3V
15	GND	P	Digital Ground
16	STBY_3V3	P	Stand by 3.3V
17			
18	STBY_3V3	P	Stand by 3.3V
19			
20			
21	GND	P	Digital Ground
22			
23			
24			
25			

Pin #	ECHO-BOARD Signal	Type	Description
26			
27	GND	P	Digital Ground
28			
29			
30			
31			
32			
33	GND	P	Digital Ground
34	USBH_PCIE_B_DP	DSIO	USB2.0 Diff. Positive; Multiplexed with USBH_P4 interface
35			
36	USBH_PCIE_B_DN	DSIO	USB2.0 Diff. Negative; Multiplexed with USBH_P4 interface
37			
38	PCIE2_DEVSLP#	I	Device Sleep. Connected to Test Point
39	GND	P	Digital Ground
40	I2C_PM_CK(I2C2_SCL)	I	I2C #2 Clock, 1V8 I/O
41	PCIE_B_CRXM	DSO	PCIe Transmit Lane Diff. Negative
42	I2C_PM_CK(I2C2_SDA)	IO	I2C #2 Data, 1V8 I/O
43	PCIE_B_CRXP	DSO	PCIe Transmit Lane Diff. Positive
44			
45	GND	P	Digital Ground
46			
47	SMR95_PCIE_B_TXN	DSI	PCIe Receive Lane Diff. Negative
48			
49	SMR95_PCIE_B_TXP	DSI	PCIe Receive Lane Diff. Positive
50	SMR95_PCIE_B_RST#_3V3	I	PCIe Port n Reset signal.
51	GND	P	Digital Ground
52	SMR95_PCIE_B_CKREQ#_3V3	O	M.2 Clock request. Connected to PCIe reference clock generator.
53	SMR95_PCIE_B_REFCK-	DSI	PCIe Clock Diff. Negative; 100MHz HCSL, generated from SOM
54	PCIE2_WAKE_B	O	PCIe wake signal
55	SMR95_PCIE_B_REFCK+	DSI	PCIe Clock Diff. Positive; 100MHz HCSL, generated from SOM
56			
57	GND	P	Digital Ground
58			
59-66 M-Key			
67			
68	PCIE2_32K	I	32.768 kHz clock supply input. Connected to Test Point
69	PCIE2_PEDET	I	STBY_3V3 PU
70	STBY_3V3	P	Stand by 3.3V
71	GND	P	Digital Ground
72	STBY_3V3	P	Stand by 3.3V
73	GND	P	Digital Ground
74	STBY_3V3	P	Stand by 3.3V
75	GND	P	Digital Ground
S1	GND	P	Digital Ground
S2	GND	P	Digital Ground

6.4.4 Ethernet

The ECHO-BOARD supports 3 Ethernet interfaces as follows:

1. ETH0, 10/100/1000BaseT. RJ45 connector – J27
2. ETH1, 10/100/1000BaseT. RJ45 connector – J26
3. ETH2, 10Gb Ethernet. SFP+ connector – J23 & J25

SOMs capability is as follows:

- VAR-SMARC-MX8M-PLUS supports interfaces 1,2
- TBD supports all

6.4.4.1 10/100/1000BaseT RJ45 Connector Pin-out (J27)

Table 6-8 10/100/1000BaseT RJ45 Connector Pin-out (J27)

Pin #	ECHO-BOARD Signal	Type	Description
L1	BASE_PER_3V3	O	Activity LED Anode;
L2	ETH0_LED_ACT	P	Activity LED Cathode;
L4	ETH0_LED_LINK_1000	IO	Link 10/100 LED Anode;
			Link 1000 LED Cathode;
L5	ETH0_LED_LINK_100	IO	Link 10/100 LED Cathode;
			Link 1000 LED Anode;
R1	TCT3	O	Primary transformer common pin
R2	ETH0_MDI_C_M	DSIO	Bi-directional diff. pair C negative
R3	ETH0_MDI_C_P	DSIO	Bi-directional diff. pair C positive
R4	ETH0_MDI_B_P	DSIO	Bi-directional diff. pair B positive
R5	ETH0_MDI_B_M	DSIO	Bi-directional diff. pair B negative
R6	TCT2	O	Primary transformer common pin
R7	TCT4	O	Primary transformer common pin
R8	ETH0_MDI_D_P	DSIO	Bi-directional diff. pair D positive
R9	ETH0_MDI_D_M	DSIO	Bi-directional diff. pair D negative
R10	ETH0_MDI_A_M	DSIO	Bi-directional diff. pair A negative
R11	ETH0_MDI_A_P	DSIO	Bi-directional diff. pair A positive
R12	TCT1	O	Primary transformer common pin
SH1	GND_EARTH	P	EARTH
SH2	GND_EARTH	P	EARTH

6.4.4.2 10/100/1000BaseT RJ45 Connector Pin-out (J26)

Table 6-9 10/100/1000BaseT RJ45 Connector Pin-out (J26)

Pin #	ECHO_BOARD Signal	Type	Description
L1	BASE_PER_3V3	O	Activity LED Anode;
L2	ETH1_LED_ACT	P	Activity LED Cathode;
L4	ETH1_LED_LINK_1000	IO	Link 10/100 LED Anode;
			Link 1000 LED Cathode;
L5	ETH1_LED_LINK_100	IO	Link 10/100 LED Cathode;
			Link 1000 LED Anode;
R1	TCT3	O	Primary transformer common pin
R2	ETH1_MDI_C_M	DSIO	Bi-directional diff. pair C negative
R3	ETH1_MDI_C_P	DSIO	Bi-directional diff. pair C positive
R4	ETH1_MDI_B_P	DSIO	Bi-directional diff. pair B positive
R5	ETH1_MDI_B_M	DSIO	Bi-directional diff. pair B negative
R6	TCT2	O	Primary transformer common pin
R7	TCT4	O	Primary transformer common pin
R8	ETH1_MDI_D_P	DSIO	Bi-directional diff. pair D positive
R9	ETH1_MDI_D_M	DSIO	Bi-directional diff. pair D negative
R10	ETH1_MDI_A_M	DSIO	Bi-directional diff. pair A negative
R11	ETH1_MDI_A_P	DSIO	Bi-directional diff. pair A positive
R12	TCT1	O	Primary transformer common pin
SH1	GND_EARTH	P	EARTH
SH2	GND_EARTH	P	EARTH

6.4.4.3 10Gb Ethernet. SFP+ connector Pin-out (J23)

Table 6-10 10/100/1000BaseT RJ45 Connector Pin-out (J23)

Pin #	ECHO-BOARD Signal	Type	Description
1	VEET	P	Transmitter Ground
2	TX_FLT	O	Transmit fault. Active low open drain
3	TX_DIS	I	Transmit disable. Active high
4	I2C_PM_DAT(I2C2_SDA)_3V3	IO	I2C #2 data. Interface module internal EEPROM
5	I2C_PM_CK(I2C2_SCL)_3V3	I	I2C #2 clock. Interface module internal EEPROM
6	SFP_PRSNT	O	Indicating module plugged in. Connected to LED (D20)
7	RS0	I	Connected to GND
8	SFP_RX_LOS	O	LOS of receive signal. Active low open drain
9	RS1	I	Connected to GND
10	VEER	P	Receiver Ground
11	VEER	P	Receiver Ground
12	ETH10G_CRX0_N	DSI	Differential transmitter input, negative
13	ETH10G_CRX0_P	DSI	Differential transmitter input, positive
14	VEER	P	Receiver Ground
15	VCCR	P	Receiver power
16	VCCT	P	Transmitter power

17	VEET	P	Transmitter Ground
18	ETH10G_CTX0_P	DSO	Differential receiver input, positive
19	ETH10G_CTX0_N	DSO	Differential receiver input, negative
20	VEET	P	Transmitter Ground

6.4.5 Audio

The ECHO-BOARD features two audio interfaces as follows:

1. Internal – Audio CODEC on SOM
2. External – Audio CODEC on Carrier

Each of these interfaces support the following features:

- Headphone
- Line-In
- Digital Mic

6.4.5.1 Internal CODEC Headphones Connector Pin-out (J16)

Table 6-11 Internal CODEC Headphone out Jack Connector Pin-out (J16)

Pin #	ECHO-BOARD Signal	Type	Description
1	AGND	AP	Analog ground return for audio.
2	HPM_LOUT_R	AO	Headphone out Left
3	HPM_ROUT_R	AO	Headphone out Right

6.4.5.2 Internal CODEC Line-In Connector Pin-out (J14)

Table 6-12 Internal CODEC Line in Jack Connector Pin-out (J14)

Pin #	ECHO-BOARD Signal	Type	Description
1	AGND	AP	Analog ground return for audio.
2	LINEM_INL_R	AI	Line-in Left input
3	LINEM_INR_R	AI	Line-in Right input

6.4.5.3 Internal Digital microphone. See ECHO-BOARD schematics U10

6.4.5.4 External CODEC Headphones Connector Pin-out (J22)

Table 6-13 External CODEC Headphone out Jack Connector Pin-out (J22)

Pin #	ECHO-BOARD Signal	Type	Description
1	AGND	AP	Analog ground return for audio.
2	HPC_LOUT_R	AO	Headphone out Left
3	HPC_ROUT_R	AO	Headphone out Right

6.4.5.5 External CODEC Line-In Connector Pin-out (J20)

Table 6-14 External CODEC Line in Jack Connector Pin-out (J20)

Pin #	ECHO-BOARD Signal	Type	Description
1	AGND	AP	Analog ground return for audio.
2	LINEC_INL_R	AI	Line-in Left input
3	LINEC_INR_R	AI	Line-in Right input

6.4.5.6 External Digital microphone. See ECHO-BOARD schematics U37

6.4.6 Serial Camera

The ECHO-BOARD supports two MIPI CSI camera sensor inputs per SMARC V2.2 spec:

- CSI0 – 2 x lanes only
- CSI1 – 2/4 x lanes

Note:

It is important to be aware that ECHO-BOARD, out of SMARC spec, can exports 4 x lanes CSI0. Please refer to ECHO-BOARD schematics and SOM datasheet.

CSI interfaces are routed to an edge connector (J24). Extension board for utilizing these interfaces can be purchased on Variscite's website.

The Camera Board Mating connector: SAMTEC 60POS 0.8mm pitch, HSEC8-130-01-SM-DV-A

6.4.6.1 Serial Camera Connector Pin-out (J24)

Table 6-15 Serial Camera Connector Pin-out (J24)

Pin #	ECHO-BOARD Signal	Type	Description
1	STBY_3V3	P	Stand by 3.3V
2	GND	P	Digital Ground
3	STBY_3V3	P	Stand by 3.3V
4	SAI5_RXC(I2C6_SDA)	IO	I2C #6 Data, port1 ctrl
5	STBY_1V8	P	Stand by 1.8V
6	SAI5_RXFS(I2C6_SCL)	IO	I2C #6 Clock, port 1 ctrl
7	STBY_1V8	P	Stand by 1.8V
8	GND	P	Digital Ground

Pin #	ECHO-BOARD Signal	Type	Description
9	GND	P	Digital Ground
10	GPIO_EXP_P0_1__GPIO1_CAM1_PWR#	O	Power down control; Active Low. GPIO Expander #1 port 1
11	CSI1_DP0	DSI	CSI Port0 Lane0, Positive
12	GPIO_EXP_P0_3__GPIO3_CAM1_RST#	O	Reset control, Active Low. GPIO Expander #1 port 1
13	CSI1_DN0	DSI	CSI Port0 Lane0, Negative
14	CSI_P2_OPT	O	Optional discrete port1
15	GND	P	Digital Ground
16	CSI_P2_SYNC	O	Sync signal port1
17	CSI1_CKP	DSI	CSI Port0 Clock, Positive
18	GND	P	Digital Ground
19	CSI1_CKN	DSI	CSI Port0 Clock, Negative
20	CSI_P2_TRIG	I	Trigger port1
21	GND	P	Digital Ground
22	GND	P	Digital Ground
23	CSI1_DP1	DSI	CSI Port0 Lane1, Positive
24	CSI2_DN3	DSI	CSI Port1 Lane3, Negative
25	CSI1_DN1	DSI	CSI Port0 Lane1, Negative
26	CSI2_DP3	DSI	CSI Port1 Lane3, Positive
27	GND	P	Digital Ground
28	GND	P	Digital Ground
29	CSI1_DP2	DSI	CSI Port0 Lane2, Positive
30	CSI2_DN2	DSI	CSI Port1 Lane2, Negative
31	CSI1_DN2	DSI	CSI Port0 Lane2, Negative
32	CSI2_DP2	DSI	CSI Port1 Lane2, Positive
33	GND	P	Digital Ground
34	GND	P	Digital Ground
35	CSI1_DP3	DSI	CSI Port0 Lane3, Positive
36	CSI2_DN1	DSI	CSI Port1 Lane1, Negative
37	CSI1_DN3	DSI	CSI Port0 Lane3, Negative
38	CSI2_DP1	DSI	CSI Port1 Lane1, Positive
39	GND	P	Digital Ground
40	GND	P	Digital Ground
41	CSI_P1_TRIG	I	Trigger port0
42	CSI2_CKN	DSI	CSI Port1 Clock, Negative
43	GND	P	Digital Ground
44	CSI2_CKP	DSI	CSI Port1 Clock, Positive
45	CSI_P1_SYNC	O	Sync signal port0
46	GND	P	Digital Ground
47	CSI_P1_OPT	O	Optional discrete port0
48	CSI2_DN0	DSI	CSI Port1 Lane0, Negative
49	GPIO_EXP_P0_2__GPIO2_CAM0_RST#	O	Reset control, Active Low. GPIO Expander #1 port0
50	CSI2_DP0	DSI	CSI Port1 Lane0, Positive
51	GPIO_EXP_P0_0__GPIO0_CAM0_PWR#	O	Power down control, Active Low. GPIO Expander #1 port0

Pin #	ECHO-BOARD Signal	Type	Description
52	GND	P	Digital Ground
53	GND	P	Digital Ground
54	STBY_1V8	P	Stand by 1.8V
55	I2C3_SCL(I2C3_SCL)	IO	I2C #3 Clock
56	STBY_1V8	P	Stand by 1.8V
57	I2C3_SDA(I2C3_SDA)	IO	I2C #3 Data
58	STBY_3V3	P	Stand by 3.3V
59	GND	P	Digital Ground
60	STBY_3V3	P	Stand by 3.3V

6.4.7 Display

The ECHO-BOARD supports 4 different display interfaces as follows:

1. LVDS
2. MIPI-DSI
3. HDMI
4. Display Port -TBD

6.4.7.1 LVDS

ECHO-BOARD support dual-Link LVDS interface.
The interface is exposed using two Variscite's standard 20 pin Headers (J8, J10). Fourth data bit of each interface is extended using additional 2 pin connectors (J9, J11).
J8 is used for connecting Variscite's standard 7" LVDS LCD screen.

6.4.7.2 LVDS CH0 Connector Pin-out (J10) – Prim. Display

Table 6-16 LVDS Channel 0 Connector Pin-out (J10)

Pin #	ECHO-BOARD Signal	Type	Description
1	LCD0_3V3	P	LCD power 3.3V
2	LCD0_3V3	P	LCD power 3.3V
3	GND	P	Digital Ground
4	GND	P	Digital Ground
5	DSI_LVDS0_TX0_CM_N	DSO	LVDS Data0 Diff. Negative
6	DSI_LVDS0_TX0_CM_P	DSO	LVDS Data0 Diff. Positive
7	GND	P	Digital Ground
8	DSI_LVDS0_TX1_CM_N	DSO	LVDS Data1 Diff. Negative
9	DSI_LVDS0_TX1_CM_P	DSO	LVDS Data1 Diff. Positive
10	GND	P	Digital Ground
11	DSI_LVDS0_TX2_CM_N	DSO	LVDS Data2 Diff. Negative
12	DSI_LVDS0_TX2_CM_P	DSO	LVDS Data2 Diff. Positive
13	GND	P	Digital Ground
14	DSI_LVDS0_CLK_CM_N	DSO	LVDS Clock Diff. Negative

Pin #	ECHO-BOARD Signal	Type	Description
15	DSI_LVDS0_CLK_CM_P	DSO	LVDS Clock Diff. Positive
16	GND	P	Digital Ground
17	BKLT_5V	P	Backlight LED 5V power
18	BKLT_5V	P	Backlight LED 5V power
19	SPDIF_EXT_CLK(PWM1_OUT)_3V3	IO	Backlight Brightness Control
20	GND	P	Digital Ground

6.4.7.3 LVDS CH0 Data3 Extension Connector Pin-out (J11)

Table 6-17 LVDS Channel 0 Data3 Connector Pin-out (J11)

Pin #	ECHO-BOARD Signal	Type	Description
1	DSI_LVDS0_TX3_CM_P	DSO	LVDS Data3 Diff. Positive
2	DSI_LVDS0_TX3_CM_N	DSO	LVDS Data3 Diff. Negative

Note:

It is important to be aware that some SOMs assemblies expose native 4 lanes MIPI-DSI instead of LVDS CH0. Please refer to ECHO-BOARD schematics and SOM datasheet.

6.4.7.4 LVDS CH1 Connector Pin-out (J8) – Sec. Display

Table 6-18 LVDS Channel 1 Connector Pin-out (J8)

Pin #	ECHO-BOARD Signal	Type	Description
1	STBY_3V3	P	Stand by power 3.3V
2	STBY_3V3	P	Stand by power 3.3V
3	GND	P	Digital Ground
4	GND	P	Digital Ground
5	LVDS1_TX0_CM_N	DSO	LVDS Data0 Diff. Negative
6	LVDS1_TX0_CM_P	DSO	LVDS Data0 Diff. Positive
7	GND	P	Digital Ground
8	LVDS1_TX1_CM_N	DSO	LVDS Data1 Diff. Negative
9	LVDS1_TX1_CM_P	DSO	LVDS Data1 Diff. Positive
10	GND	P	Digital Ground
11	LVDS1_TX2_CM_N	DSO	LVDS Data2 Diff. Negative
12	LVDS1_TX2_CM_P	DSO	LVDS Data2 Diff. Positive
13	GND	P	Digital Ground
14	LVDS1_CLK_CM_N	DSO	LVDS Clock Diff. Negative
15	LVDS1_CLK_CM_P	DSO	LVDS Clock Diff. Positive
16	GND	P	Digital Ground
17	VCC_5V	P	Backlight LED 5V power
18	VCC_5V	P	Backlight LED 5V power
19	GPIO1_IO11(PWM2_OUT)_3V3	IO	Backlight Brightness Control; GPIO1_IO11
20	GND	P	Digital Ground

6.4.7.5 LVDS CH1 Data3 Extension Connector Pin-out (J9)

Table 6-19 LVDS Channel 0 Data3 Connector Pin-out (J9)

Pin #	ECHO-BOARD Signal	Type	Description
1	LVDS1_TX3_CM_P	DSO	LVDS Data3 Diff. Positive
2	LVDS1_TX3_CM_N	DSO	LVDS Data3 Diff. Negative

6.4.7.6 MIPI-DSI

DSI is exposed in two different ways:

1. Via J10 as described above in section 6.4.7.2
2. Via J7 as described below in section 6.4.7.7

6.4.7.7 MIPI-DSI Pin-out for DART-MX8M-PLUSE (J7)

Table 6-20 MIPI-DSI Pin-out connector (J7)

Pin #	ECHO-BOARD Signal	Type	Description
1	I2C_GP_DAT(I2C4_SDA)_3V3	IO	I2C #4 Data
2	I2C_GP_CK(I2C4_SCL)_3V3	IO	I2C #4 Clock
3	STBY_3V3	P	Stand by power 3.3V
4	STBY_3V3	P	Stand by power 3.3V
5	GND	P	Digital Ground
6	GND	P	Digital Ground
7	DSI_D0_N	DSO	DSI Data0 Diff. Negative
8	DSI_D0_P	DSO	DSI Data0 Diff. Positive
9	GND	P	Digital Ground
10	DSI_D1_N	DSO	DSI Data1 Diff. Negative
11	DSI_D1_P	DSO	DSI Data1 Diff. Positive
12	GND	P	Digital Ground
13	DSI_D2_N	DSO	DSI Data2 Diff. Negative
14	DSI_D2_P	DSO	DSI Data2 Diff. Positive
15	GND	P	Digital Ground
16	DSI_CLK_N	DSO	DSI Clock Diff. Negative
17	DSI_CLK_P	DSO	DSI Clock Diff. Positive
18	GND	P	Digital Ground
19	STBY_5V	P	Backlight LED 5V power
20	STBY_5V	P	Backlight LED 5V power
21	SPDIF_EXT_CLK(PWM1_OUT)_3V3	O	Backlight Brightness Control
22	GND	P	Digital Ground
23	DSI_D3_N	DSO	DSI Data3 Diff. Negative
24	DSI_D3_P	DSO	DSI Data3 Diff. Positive

Note:

It is important to be aware that future SMARC SOM will have the assembly option to route DisplayPort interface instead of J7 MIPI-DSI interface (via MIPI-DSI to DP bridge). Please refer to ECHO-BOARD schematics and TBD SOM datasheet.

6.4.7.8 HDMI

HDMI interface is routed through mini-HDMI connector (Type-C).

6.4.7.9 mini-HDMI Connector Pin-out (J13)

Table 6-21 mini-HDMI Connector Pin-out (J13)

Pin #	ECHO-BOARD Signal	Type	Description
1	GND	P	Digital Ground
2	HDMI_TX2_CM_P	DSO	HDMI TMDS Diff. Data 2, Positive
3	HDMI_TX2_CM_N	DSO	HDMI TMDS Diff. Data 2, Negative
4	GND	P	Digital Ground
5	HDMI_TX1_CM_P	DSO	HDMI TMDS Diff. Data 1, Positive
6	HDMI_TX1_CM_N	DSO	HDMI TMDS Diff. Data 1, Negative
7	GND	P	Digital Ground
8	HDMI_TX0_CM_P	DSO	HDMI TMDS Diff. Data 0, Positive
9	HDMI_TX0_CM_N	DSO	HDMI TMDS Diff. Data 0, Negative
10	GND	P	Digital Ground
11	HDMI_TXC_CM_P	DSO	HDMI TMDS Diff. Clock, Positive
12	HDMI_TXC_CM_N	DSO	HDMI TMDS Diff. Clock, Negative
13	GND	P	Digital Ground
14	HDMI_CEC_3V3	IO	HDMI Consumer Electronics Control, 1 Wire Serial, Bidirectional
15	HDMI_DDC_SCL_5V	O	I2C Clock for HDMI DDC
16	HDMI_DDC_SDA_5V	IO	I2C Data for HDMI DDC
17			
18	HDMI_5V_CON	P	HDMI 5V
19	HDMI Hot Plug Detect	I	HDMI Hot Plug Detect

6.4.7.10 mini-DisplayPort - TBD

6.4.8 Capacitive Touch

ECHO-BOARD provides a capacitive Touch interface exposed to an FFC/FPC connector for connecting to Variscite's standard 7" Capacitive touch LCD screen.

6.4.8.1 Capacitive Touch Panel Connector Pin-out (J5)

Table 6-22 Capacitive Touch Panel Connector Pin-out (J5)

Pin #	ECHO-BOARD Signal	Type	Description
1	EXP_CAPTOUCH_RST_B	O	Capacitive Touch Reset, Active Low GPIO Expander #1 port 0
2	I2C_GP_DAT(I2C4_SDA)_3V3	IO	I2C #4 Data
3	I2C_GP_CK(I2C4_SCL)_3V3	O	I2C #4 Clock
4	CAP_TOUCH_INT#	IO	Capacitive Touch Interrupt; Active Low; GPIO1_IO14
5	STBY_3V3	P	Stand by 3.3V
6	GND	P	Digital Ground

6.4.9 USB - Debug

The ECHO-BOARD exposes the debug UART2 interface. The signals are driven by an on-board UART-to-USB Bridge and exposed to a USB-C connector.

6.4.9.1 USB Debug Connector Pin-out (J31)

Table 6-23 USB Debug Connector Pin-out (J31)

Pin #	ECHO_BOARD Signal	Type	Description
A1	GND	P	Ground return
A2			
A3			
A4	DEBUG_VBUS_C	P	Bus power
A5	DBG_CC1	IO	Pulled down to GND
A6	USB_DEBUG_DP	DSIO	Non-SuperSpeed diff. pair, pos. 1, positive
A7	USB_DEBUG_DN	DSIO	Non-SuperSpeed diff. pair, pos. 1, negative
A9	DEBUG_VBUS_C	P	Bus power
A10			
A11			
A12	GND	P	Digital Ground
B1	GND	P	Digital Ground
B2			
B3			
B4	DEBUG_VBUS_C	P	Bus power
B5	DBG_CC2	IO	Pulled down to GND
B6	USB_DEBUG_DP	DSIO	Non-SuperSpeed diff. pair, pos. 2, positive
B7	USB_DEBUG_DM	DSIO	Non-SuperSpeed diff. pair, pos. 2, negative
B8			
B9	DEBUG_VBUS_C	P	Bus power

Pin #	ECHO_BOARD Signal	Type	Description
B10			
B11			
B12	GND	P	Digital Ground
SH1	GND	P	SHIELD pin reference
SH2	GND	P	SHIELD pin reference
SH3	GND	P	SHIELD pin reference
SH4	GND	P	SHIELD pin reference

6.4.10 I2C, BT/WIFI, CAN FD & SPDIF

The ECHO-BOARD exposes I2C, BT/WIFI, CAN FD and SPDIF interfaces. Signals are routed to a standard 20 pin Header. Some of these interfaces are used or shared by other functions. Please see note below this table for more details.

6.4.10.1 I2C, BT/WIFI, CAN FD & SPDIF Connector Pin- out (J6)

Table 6-24 I2C, BT/WIFI CAN FD & SPDIF Connector Pin-out (J6)

Pin #	ECHO-BOARD Signal	Type	Description
1	BT_DEV_WAKE	O	BT device wake signal
2	BASE_PER_3V3	P	Base board 3V3
3	BT_HOST_WAKE	I	BT host wake signal
4	CAN1_H	IO	CAN Bus High side, port0
5	WIFI_HOST_WAKE	I	WIFI host wake signal
6	CAN1_L	IO	CAN Bus Low side, port0
7	WB_KILL_1V8	O	WB kill signal
8	CAN2_H	IO	CAN Bus High side, port1
9	I2C2_SDA(ECSPI1_SS0)	IO	I2C Data #2
10	CAN2_L	IO	CAN Bus Low side, port1
11	I2C1_SCL(ECSPI1_SCLK0)	IO	I2C Clock #1
12	SPDIF_TX(FLEXCAN1_TX)_3V3	IO	SPDIF Transmit Data. Refer to note below
13	I2C1_SDA(ECSPI1_MOSI)	IO	I2C Data #1
14	SPDIF_RX(FLEXCAN1_RX)_3V3	IO	SPDIF Receive Data. Refer to note below
15	I2C2_SCL(ECSPI1_MISO)	IO	I2C Clock #2
16	HDMI_CEC(FLEXCAN2_TX)_3V3	IO	HDMI Consumer Electronics Control.
17	JTAG_MOD	O	Enter JTAG mode
18	SAI5_MCLK(CAN2_RX)_3V3	IO	SAI5 Master Clock
19	GND	P	Digital ground
20	VCC_5V	P	Base board 5V

Note:

SPDIF_RX, SPDIF_TX, HDMI_CEC & SAI5_MCLK are connected by serial resistors to CAN-FD interface.
ECSPI1 for the BT and WIFI module in WBE assembly.
For more details, please refer to ECHO-BOARD schematics and specific SOM datasheet.

6.4.11 UART, NAND/QSPI & ETH Ctrl

ECHO-BOARD exposes UART, NAND/QSPI & ETH Ctrl. Signals are routed to a standard 24 pins Header. Some of these interfaces are used or shared by other functions.
Please see note below this table for more details.

6.4.11.1 Connector Pin- out (J15)

Table 6-25 UART, NAND/QSPI and ENET Ctrl Connector Pin-out (J15)

Pin #	ECHO-BOARD Signal	Type	Description
1	GND	P	Digital ground
2	BASE_PER_1V8	P	Base board 1.8V
3	ECSPI2_SS0(NAND_CE0_B)	IO	SPI2 Slave Select; Active Low
4	UART1_RXD(UART1_RXD)	IO	UART1 Receive
5	ECSPI2_SCLK(NAND_ALE)	IO	SPI2 Serial Clock
6	UART1_TXD(UART1_TXD)	IO	UART1 Transmit
7	ECSPI2_MOSI(NAND_DATA00)	IO	SPI2 Master Out Slave In
8	UART3_RXD(UART1_CTS)	IO	UART3 Receive
9	ECSPI2_MISO(NAND_DATA01)	IO	SPI2 Master in Slave out
10	UART3_TXD(UART1_RTS)	IO	UART3 Transmit
11	NAND_DATA02(QSPI_A_DATA2)	IO	QSPI data2
12	UART4_TXD(UART4_TXD)	IO	UART4 Transmit
13	NAND_DATA03(QSPI_A_DATA3)	IO	QSPI data3
14	UART4_RXD(UART4_RXD)	IO	UART4 Receive
15	NAND_DQS	IO	QSPI Strobe
16	ECSPI1_MOSI(UART3_TXD)	IO	SPI1 Master out Slave in
17	ENET_MDC	O	ENET Management Clock
18	ECSPI1_SCLK(UART3_RXD)	IO	SPI1 Serial Clock
19	ENET_MDIO	IO	ENET Management Data
20	ECSPI1_MISO(UART3_CTS)	IO	SPI1 Master in Slave out
21	ETH0_INT_IN	I	ETH PHY0 interrupt signal
22	ECSPI1_SS0(UART3_RTS)	IO	SPI1 Slave Select; Active Low
23	ETH1_INT_IN	I	ETH PHY1 interrupt signal
24	GND	P	Digital ground

Note:

For NAND/QSP and other functions of these pins refer to the SOM data sheet
UART3(ECSPI1) is used for the BT and WIFI module in WBE assembly.
For more details, please refer to ECHO-BOARD schematics and specific SOM datasheet.

6.4.12 GPIO

The ECHO-BOARD exports alternate GPIO's through a standard 10 pins Header.

6.4.12.1 GPIO Pin-out J12

Table 6-26 GPIOs Connector Pin-out (J12)

Pin #	ECHO_BOARD Signal	Type	Description
1	SAI1_RXC(ENET1_1588_EVENT0_OUT)_3V3	O	GPIO4_IO01
2	GPIO1_IO07	IO	GPIO1_IO07
3	GPIO1_IO09(ENET_QOS_1588_EVENT0_ OUT)_3V3	O	GPIO1_IO09
4	GPIO1_IO06	IO	GPIO1_IO06
5	GPIO1_IO00	IO	GPIO1_IO00
6	GPIO1_IO15(CCM_CLKO2)	IO	GPIO1_IO15
7	GPIO1_IO03	IO	GPIO1_IO03
8	SD2_WP	O	SD card WP signal
9	GPIO1_IO01	IO	GPIO1_IO01
10	GND	P	Digital Ground

6.5 User Interfaces

6.5.1 Control Buttons

6.5.1.1 Power Switch (SW12)

The Power Switch SW12 Connect/Isolate the DC Power input to the ECHO-BOARD.

6.5.1.2 Boot Select (SW7)

The Boot select switch SW7 sets the SOM boot source & sequence. Refer to ECH0-BOARD and the SOM data sheet for detailed Boot description. The table below describes the boot options.

Table 6-27 Boot Options (SW7)

SW4 – Force Recovery	SW3 – BOOT SEL2	SW2 – BOOT SEL1	SW1 -BOOT SEL0	Device
Off	On	On	On	QSPI
Off	On	On	Off	SD Card
Off	On	Off	Off	SPI
Off	Off	Off	On	eMMC
On	X	X	X	USB Serial Download

6.5.1.3 User Buttons (SW5, SW6, SW8, SW10)

SW5, SW6, SW8 and SW10 are User Buttons connected to GPIO Expander #1 ports 4-7 for general purpose usage. In Linux release they can be configured, e.g., as Left, Enter, and Right Buttons in the DTS file.

6.5.1.4 Reset Button (SW9)

A press on SW9 will perform a system hardware-reset resulting in a complete power cycle of the SOMs.

6.5.1.5 ON/OFF Button (SW11)

The ON/OFF is Button supports the following:

1. **In OFF mode:** A short button press causes the internal power management state machine to change state to ON.
2. **In ON mode:** A short button press generates an interrupt (intended to initiate a software-controllable power-down).
   An approximate 5 second or more button press causes a forced OFF.
3. **In Suspend mode:** A short button press will the system to exit suspend mode.

6.5.2 LED Indications

6.5.2.1 Power-On LEDs (D23, D27, D28)

Two LED indicators used:

- **D23** indicates that the ECHO-BOARD VCC_5V power is ON
- **D27** indicates that the EHO-BOARD STBY_3V3 power is ON
- **D28** indicates that the ECHO-BOARD VCC_12V DC IN is ON.

6.5.2.2 SFP+ module present indication LED (D20) – TBD

6.5.2.3 GP LEDs (D21, D22, D24, D25)

- LEDs **D21**, **D22**, **D24** are General Purpose functionality LED controlled by GPIO Expander #1 ports 5-7.
- LED **D25** is a General-Purpose functionality LED controlled by a GPIO.

6.5.3 Power

The ECHO-BOARD is powered by a +12V power supply, connected either through a 2.0 mm power plug (J30) or alternatively through a 2 pin Terminal block (J34).

A 12V/5V fan power output is available via shrouded 2 pin header (J34). Mating Housing Molex 22-01-3027; Connector Terminal Female Molex 08-50-0114;

6.5.3.1 DC-in Jack Pin-out (J30)

Table 6-28 DC-in Jack Pin-out (J30)

Pin #	ECHO-BOARD Signal	Type	Description
1	GND	P	Power supply return
2	GND	P	Power supply return
3	VCC_12V_PJ	P	Power supply 12V
4	VCC_12V_PJ	P	Power supply 12V

6.5.3.2 DC-in Terminal Block Pin-out (J34)

Table 6-29 DC-in 2 pins Terminal Block Pin-out (J34)

Pin #	ECHO-BOARD Signal	Type	Description
1	GND	P	Power supply return
2	VCC_12V_PJ	P	Power supply 12V

6.5.3.3 DC-out FAN 5V Pin-out (J21)

Table 6-30 DC-out 5V FAN Header Pin-out (J21)

Pin #	ECHO-BOARD Signal	Type	Description
1	FAN_PWR	P	Power supply 12V/5V out ***Note: Power via Ferrite Bead***
2	GND	P	Ground Return

Note:
J21, J34 are not assembled.
ECHO-BOARD has an assembly option to connect 12V fan to J34 instead of 5V.

6.5.3.4 RTC

The Sonata-Board features 12V input LDO. It supplies 1.8V to SOMs RTC Module.
Thus, to check RTC feature, 12V input must be connected. ECHO-BOARD has an assembly option to add battery for those who wants to check it without power input.

7. Electrical Environmental Specifications

7.1 Absolute maximum electrical specifications

Table 7-1 DC Power Input absolute maximum electrical specifications

	Min	Max
Main Power Supply, DC-IN	-0.3V	20V

7.2 Operational electrical specifications

Table 7-2 DC Power Input Operational electrical specifications

	Min	Max
Main Power Supply, DC-IN	8V	18V

8. Environmental specifications

Table 8-1 Environmental specifications

	Min	Max
Commercial operating temperature range	0^0C	+70^0C
MTBF	>10kHRS	
Relative humidity, Operational	10%	90%
Relative humidity, Storage	5%	95%

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