Sonata Board 1.1C

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Disclaimer:

SchematicS are for reference only.
Variscite LTD provides no warranty for the use of these schematics.
Schematics are subject to change without notice.

Revision History

Document	Carrier	Description
1.0	1.0	New layout to support DART-MX95, DART-MX93 & DART-MX91
1.1	1.1	1. Adding DT91 & DT93 block diagrams and symbols 2. DART-MX95 V1.1 J3.48 and J3.50 GPIO swap 3. Change IO EXP. #3 (U37) address to 0x22 4. SPI contention issue - U8.16 connect to U8.1 5. Remove R172 6. Combine R1 and R2. R1 removed, R2 changed to 174K and R3 changed to 31.6K 7. Connect 3.8 LED to regulator PGOOD pin 8. Buffer enable when RGB mode is off - Connect U26.7 to U37.2 9. Put RGMII filters on clock signals only. 10. Enable SOM_SNVS power by DIP SW when DT95 11. R28 changed to 1K 12. C205 changed to 1nF - solve DT95 boot always from eMMC 13. Remove SFP CLK EMI filtre L16 14. SFP RX p/n swap 15. Replace DT95 symbols 16. Add RGB 666 LCD connector - J36 17. Solve LDO RTC issue - Replace R102 and R106 with diode - Adding 1K resistr between 12V and U24 - Replace C136 to 10uF - Add voltage divider to Q10 to protect it fom burning 18. Trusted Platform Module (TPM) U60
1.2	1.1A	1. U5, U29, U47 changed to CBTL02042BBQ,115 2. Logo updated
1.3	1.1B	1. U26 changed to NC
1.4	1.1C	1. J25 was replaced to Molex 747370010 - VCN0273 2. R127 set to NC. It interferes with the boot mode of DART-MX8M-MINI

For complete alternate function per pin
and specific SOM please refer to:
"DART_Compatibility_and_Pinout.XLS" located at:
ftp://ftp.variscite.com/DART_Compatibility

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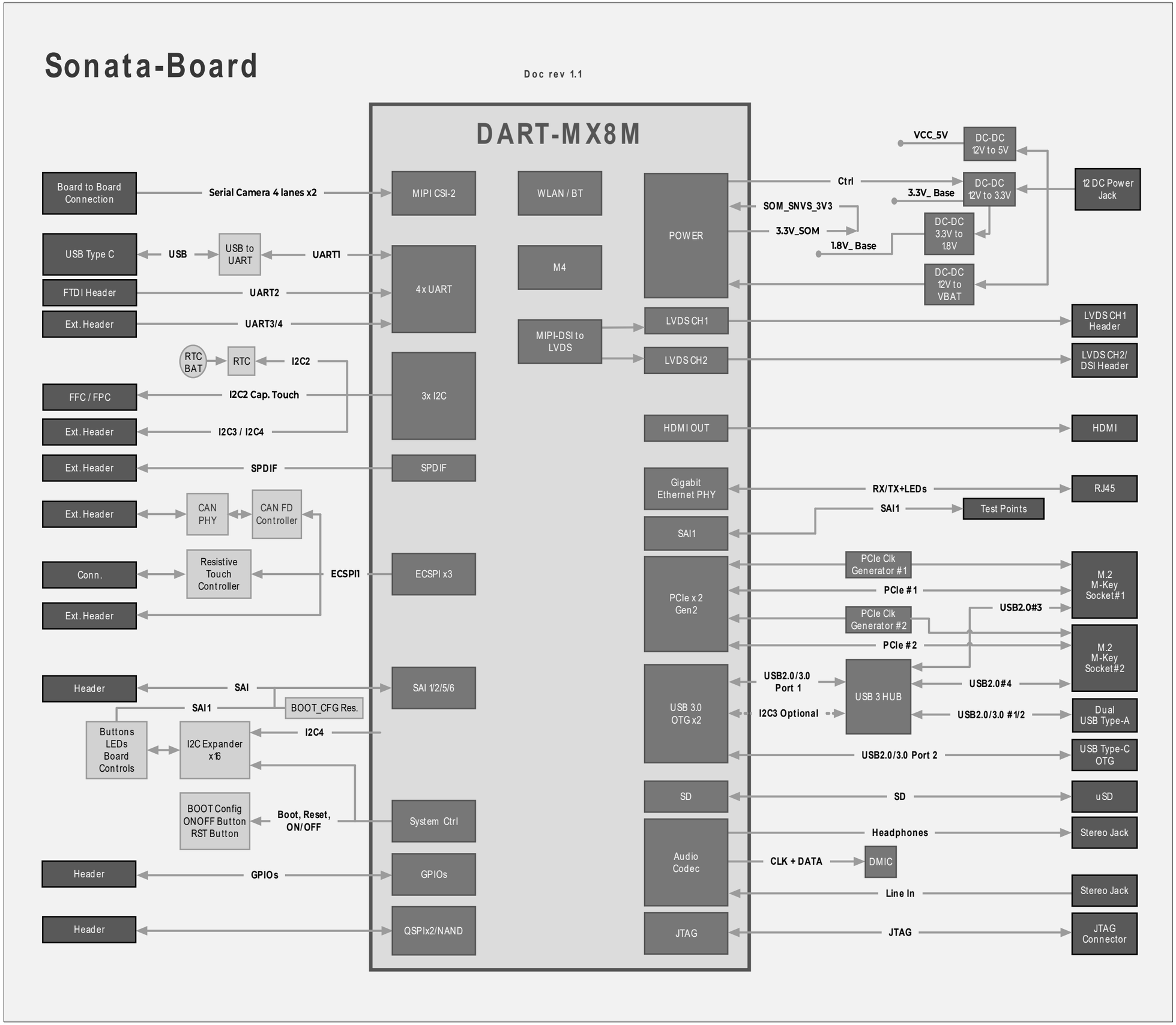
Title: 01. Cover			
Size: A3	Document Number: Sonata Board	Project: Sonata Board	Rev: R1.1C_D1.4
Designer: Shay V.		Approved By:	
Date: Wednesday, October 15, 2025		Sheet 1 of 23	

02A. Block Diagram - DART-MX8M



I2C BUS ADDRESS:

```
I2C1:   Internal to SOM

I2C2:   PU - 10K on U8
            10K on custom
        0x54 BOARD ID EEPROM Page0
        0x55 BOARD ID EEPROM Page1
        0x68 RTC
        0x38 CAPACITIVE TOUCH CTRLR
        0x3D USB-C CC Logic PTN5150AHXMP
        0x3C CSI P1 Camera (1V8) OV5640


I2C3:   PU - 5K on SOM
        0x60 SOM - Int. power ctrl.
        0x2D USB3 HUB
        0xXX Header J12

I2C4:   PU - 10K on U8
            10K on custom
        0x3C CSI P2 Camera (1V8) OV5640
        0xXX Header J12
        0xXX mPCIe J23 & J32
```

Important Notes:

1. Length match for HS signals according to SOM DS
2. USB routed as 90 ohm Diff pairs
3. PCIe/SATA routed as 85 ohm Diff pairs
4. LVDS routed as 100 ohm Diff pairs
5. Other fast changing signals routed as 50 ohm

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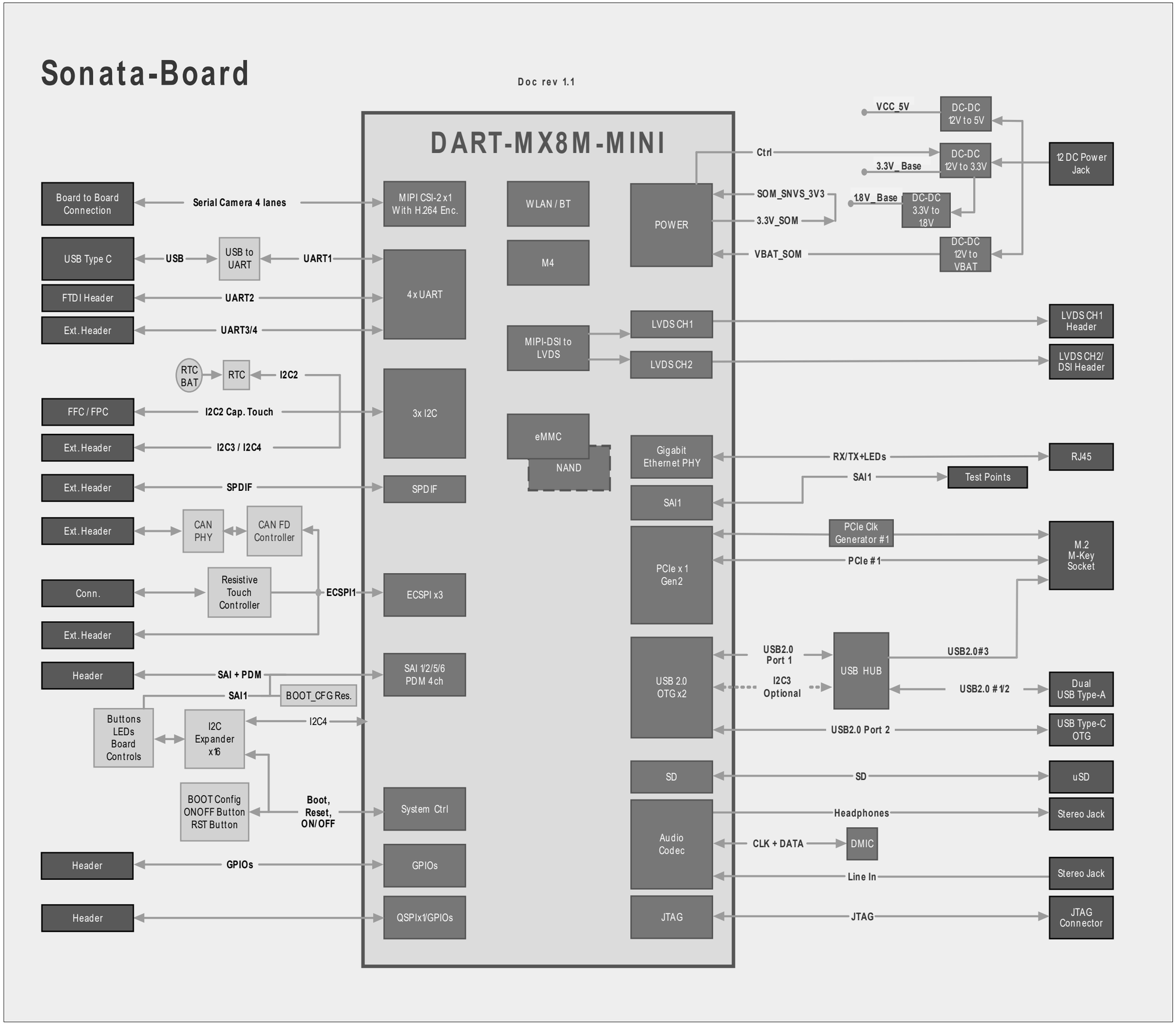
Title: 02A. Block Diagram - DART-MX8M			
Size: A3	Document Number: Sonata Board	Project: Sonata Board	Rev: R1.1C_D1.4
Designer: Shay V.		Approved By:	
Date: Sunday, October 05, 2025		Sheet 2 of 23	

02B. Block Diagram - DART-MX8M-MINI



I2C BUS ADDRESS:

```
I2C1:   Internal to SOM

I2C2:   PU - 10K on U8
            10K on custom
        0x54 BOARD ID EEPROM Page0
        0x55 BOARD ID EEPROM Page1
        0x68 RTC
        0x38 CAPACITIVE TOUCH CTRLR
        0x3D USB-C CC Logic PTN5150AHXMP
        0x3C CSI P1 Camera (1V8) OV5640


I2C3:   PU - 5K on SOM
        0x1A SOM - Int. CODEC
        0x2D USB3 HUB
        0xXX Header J12

I2C4:   PU - 10K on U8
            10K on custom
        0x3C CSI P1 Camera (1V8) OV5640
        0xXX Header J12
        0xXX mPCIe J23 & J32
```

Important Notes:

1. Length match for HS signals according to SOM DS
2. USB routed as 90 ohm Diff pairs
3. PCIe/SATA routed as 85 ohm Diff pairs
4. LVDS routed as 100 ohm Diff pairs
5. Other fast changing signals routed as 50 ohm

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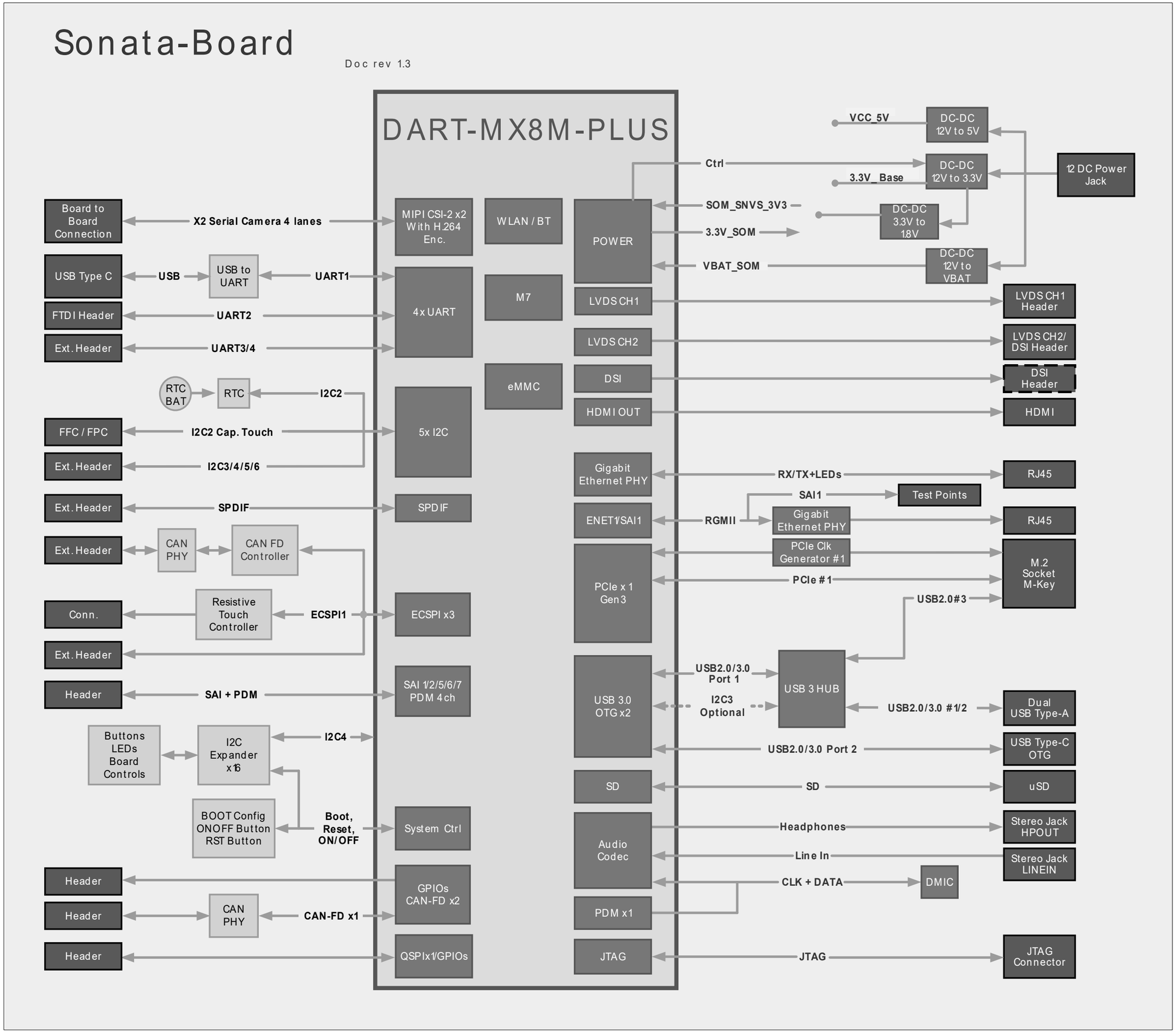
Title: 02B. Block Diagram - DART-MX8MM			
Size: A3	Document Number: Sonata Board	Project: Sonata Board	Rev: R1.1C_D1.4
Designer: Shay V.		Approved By:	
Date: Sunday, October 05, 2025		Sheet 3 of 23	

02C. Block Diagram - DART-MX8M-PLUS



I2C BUS ADDRESS:

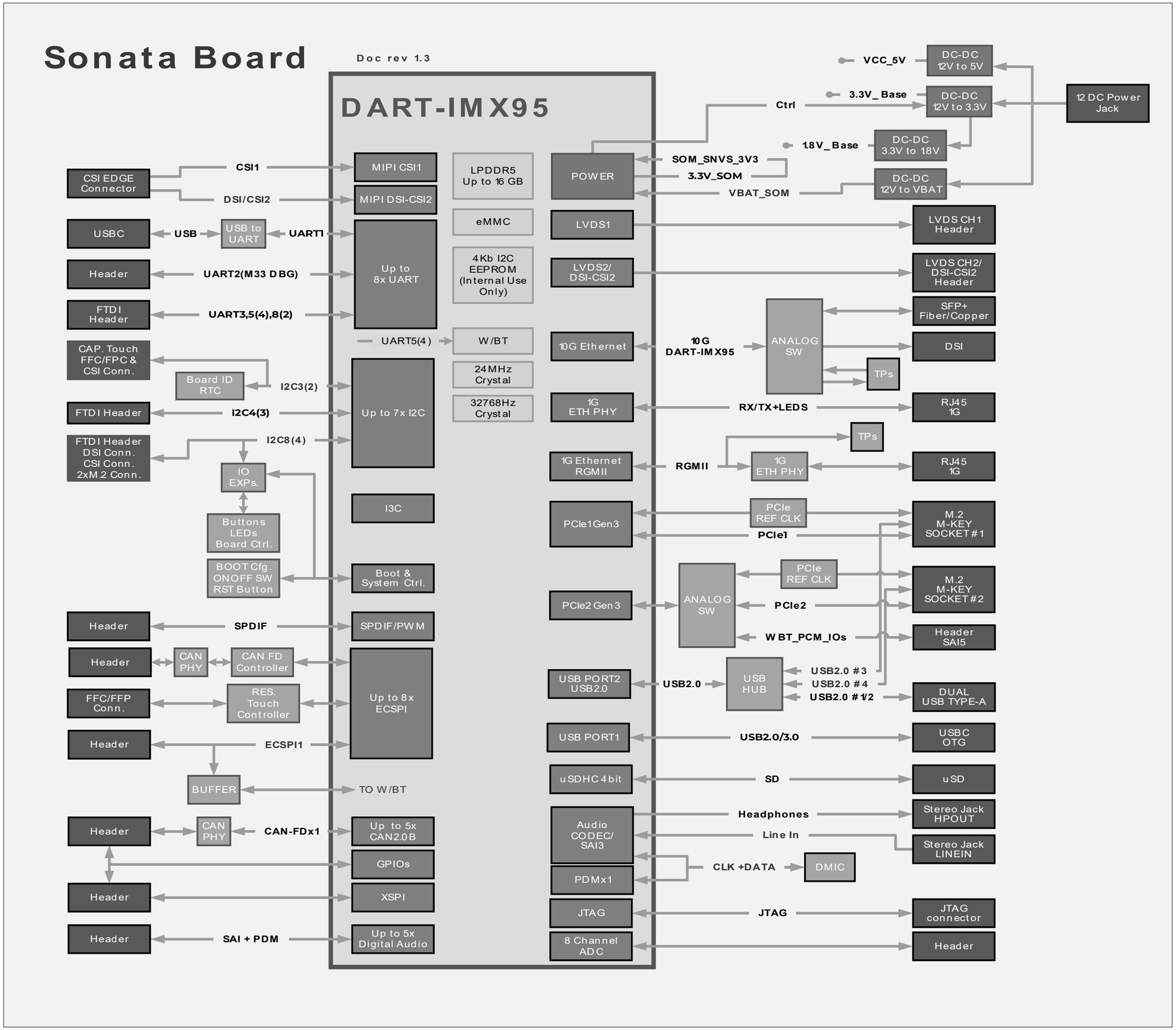
```
I2C1:   Internal to SOM

I2C2:   PU - 10K on U8
            10K on custom
        0x54 BOARD ID EEPROM Page0
        0x55 BOARD ID EEPROM Page1
        0x68 RTC
        0x38 CAPACITIVE TOUCH CTRLR
        0x3D USB-C CC Logic PTN5150AHXMP
        0x3C CSI P1 Camera (1V8) OV5640


I2C3:   PU - 5K on SOM

        0x2D USB3 HUB
        0xXX Header J12

I2C4:   PU - 10K on U8
            10K on custom
        0x3C CSI P1 Camera (1V8) OV5640
        0xXX Header J12
        0xXX mPCIe J23 & J32
```

Important Notes:

1. Length match for HS signals according to SOM DS
2. USB routed as 90 ohm Diff pairs
3. PCIe/SATA routed as 85 ohm Diff pairs
4. LVDS routed as 100 ohm Diff pairs
5. Other fast changing signals routed as 50 ohm

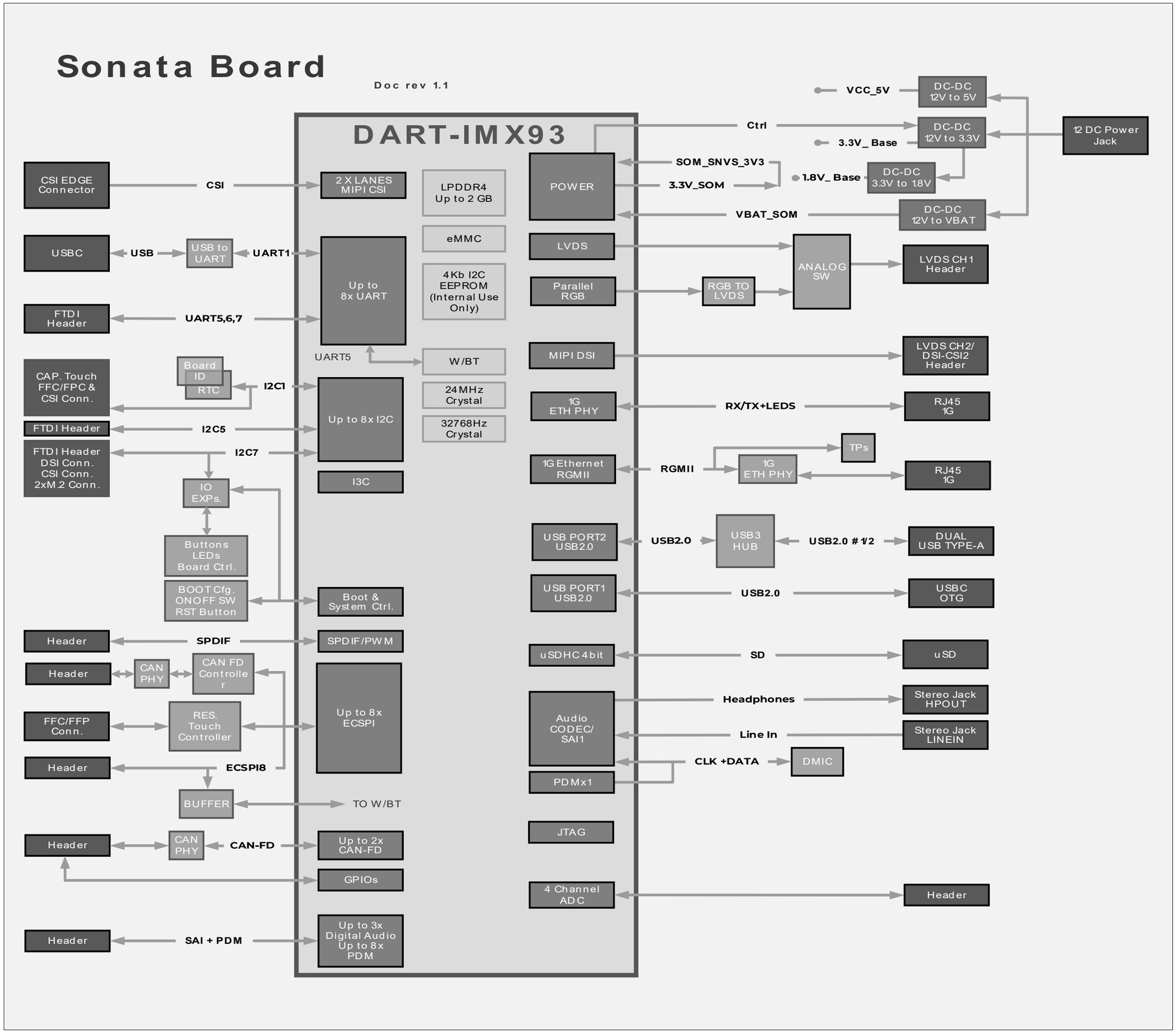
Title: 02C. Block Diagram - DART-MX8MP			
Size: A3	Document Number: Sonata Board	Project: Sonata Board	Rev: R1.1C_D1.4
Designer: Shay V.		Approved By:	
Date: Sunday, October 05, 2025		Sheet 4 of 23	

02D. Block Diagram - DART-MX95



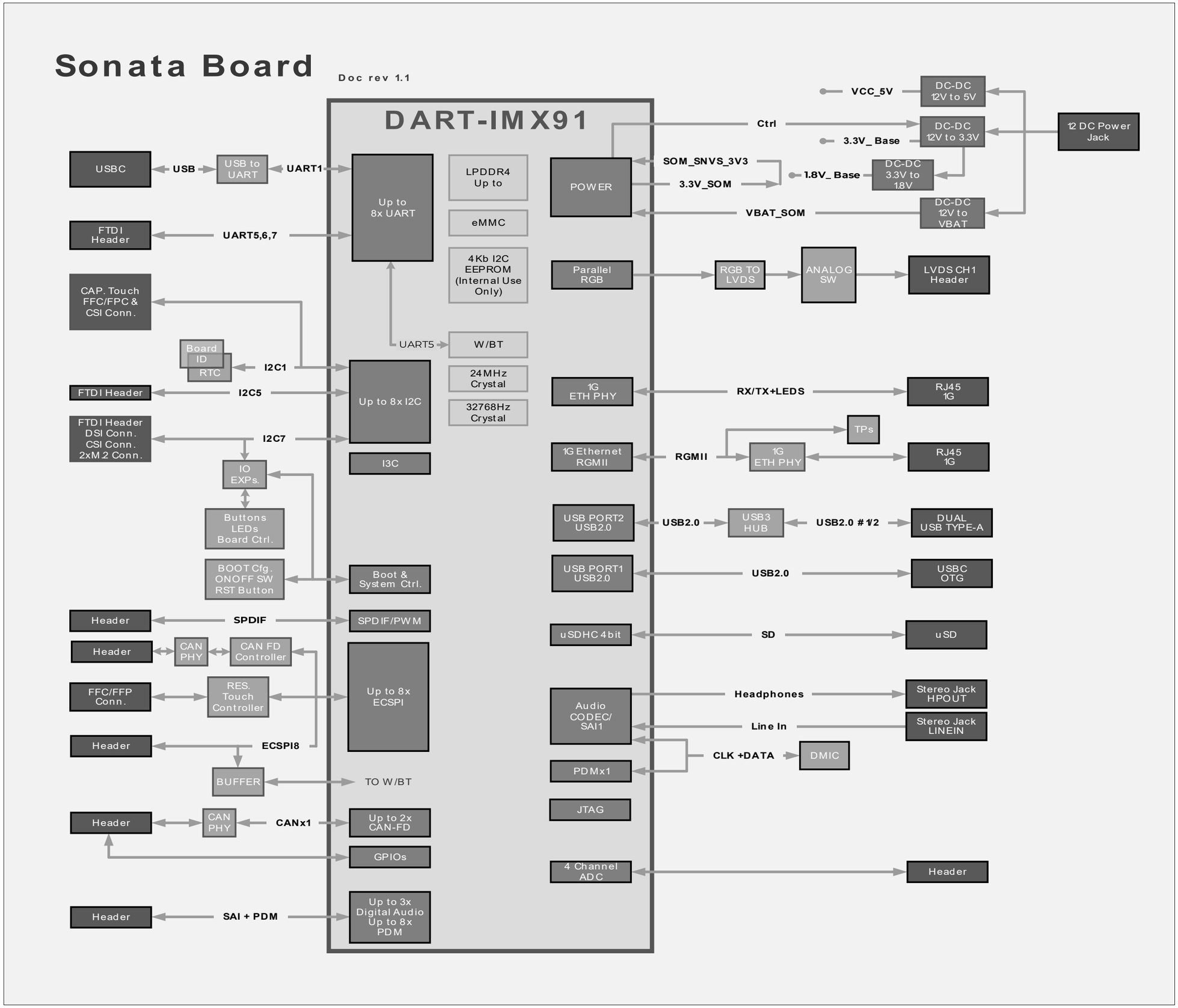
Title: 02D. Block Diagram - DART-MX95			
Size: A3	Document Number: Sonata Board	Project: Sonata Board	Rev: R1.1C_D1.4
Designer: Shay V.		Approved By:	
Date: Sunday, October 05, 2025		Sheet 5 of 23	

02E. Block Diagram - DART-MX93



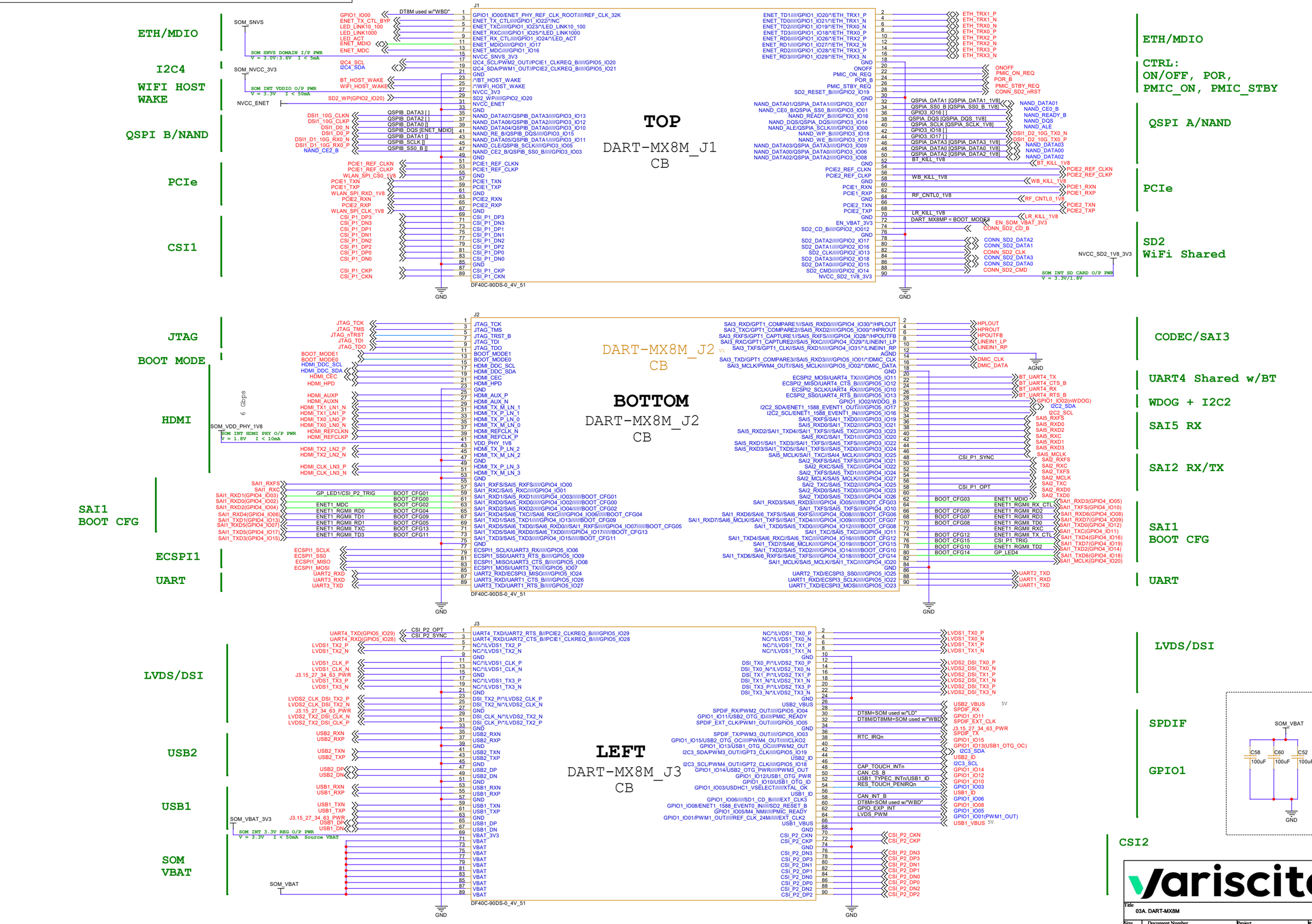
Title: 02E. Block Diagram - DART-MX93			
Size: A3	Document Number: Sonata Board	Project: Sonata Board	Rev: R1.1C_D1.4
Designer: Shay V.		Approved By:	
Date: Sunday, October 05, 2025		Sheet 6 of 23	

02F. Block Diagram - DART-MX91



Title: 02F. Block Diagram - DART-MX91			
Size: A3	Document Number: Sonata Board	Project: Sonata Board	Rev: R1.1C_D1.4
Designer: Shay V.		Approved By:	
Date: Sunday, October 05, 2025		Sheet 7 of 23	

03A - DART-MX8M Connectors



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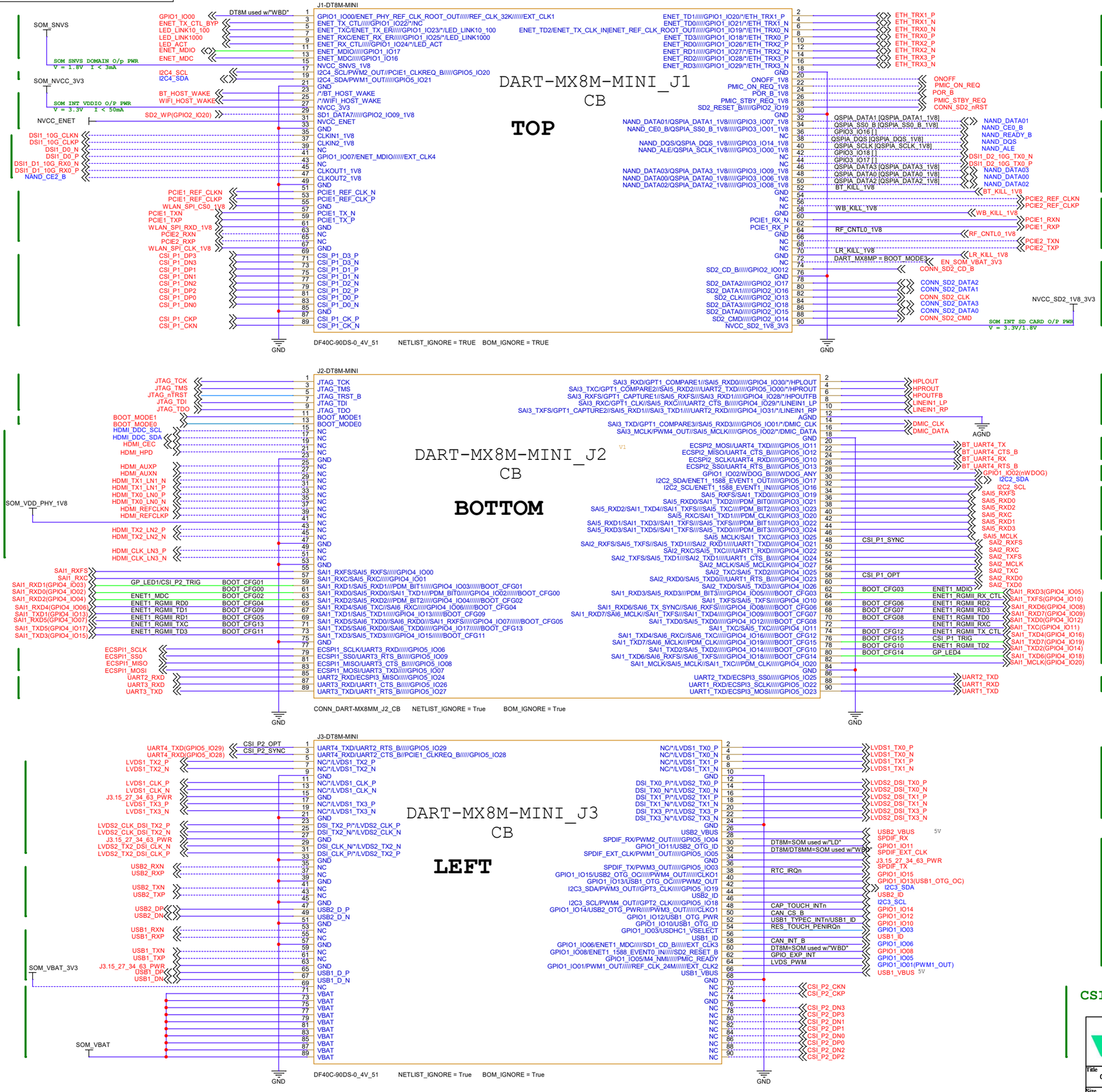
Title	03A. DART-MX8M
Size	A2
Document Number	Sonata Board
Project	Sonata Board
Rev	R1.1C_D1.4
Designer:	Shay V.
Approved By:	
Date:	Sunday, October 05, 2025
Sheet	8 of 23

03B - DART-MX8M-MINI Connectors

***** Dotted nets - Functionality differ from DART-MX8M. *****



Note: Pinname with /*/ prefix denotes a HW assy option.

variscite

Title	03B. DART-MX8M-MINI
Size	A2
Document Number	Sonata Board
Project	Sonata Board
Rev	R1.1C_D1.4
Designer:	Shay V.
Approved By:	
Date:	Sunday, October 05, 2025
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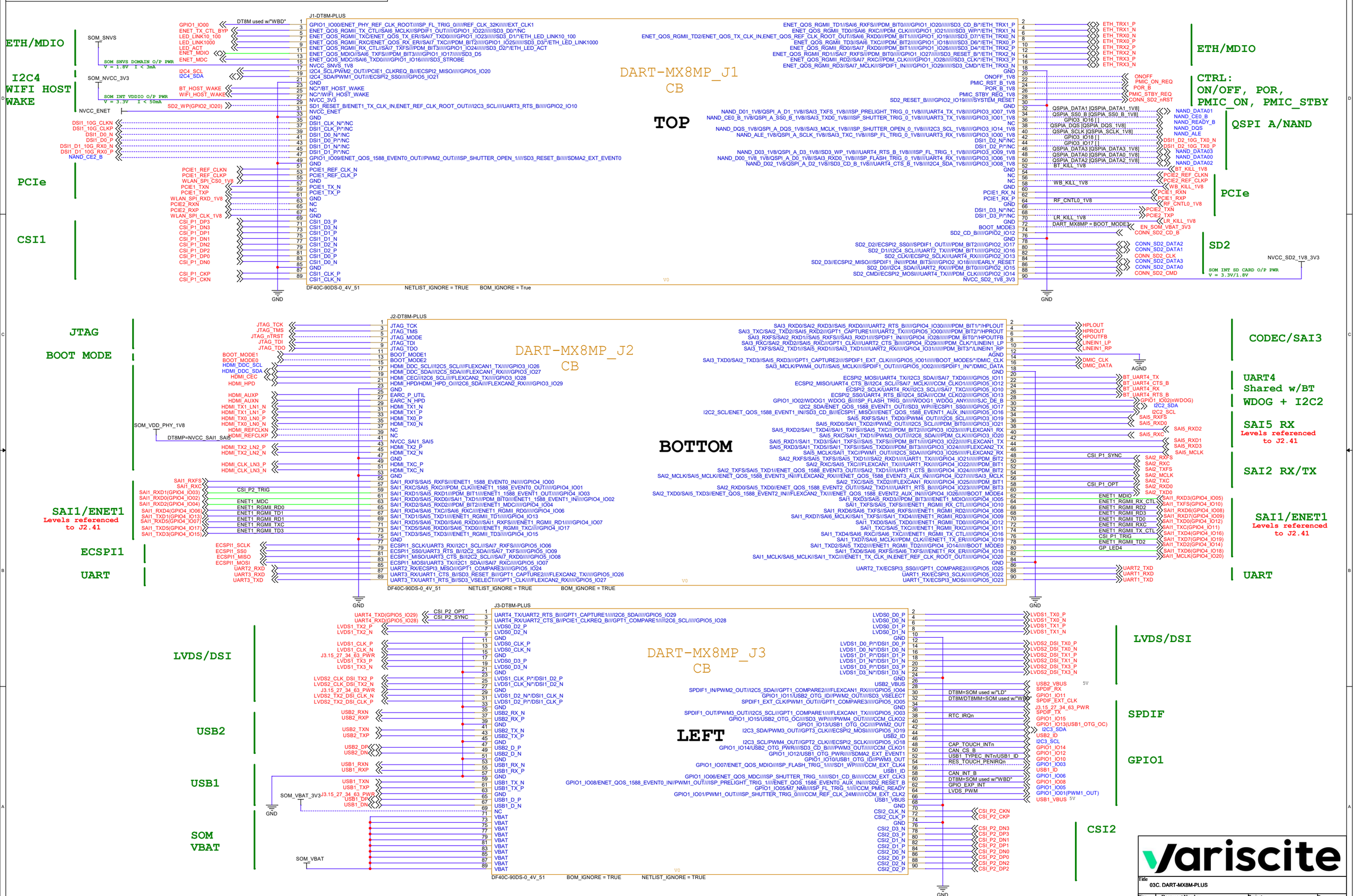
03C - DART-MX8M-PLUS Connectors

***** Dotted nets - Functionality differ from DART-MX8M. *****

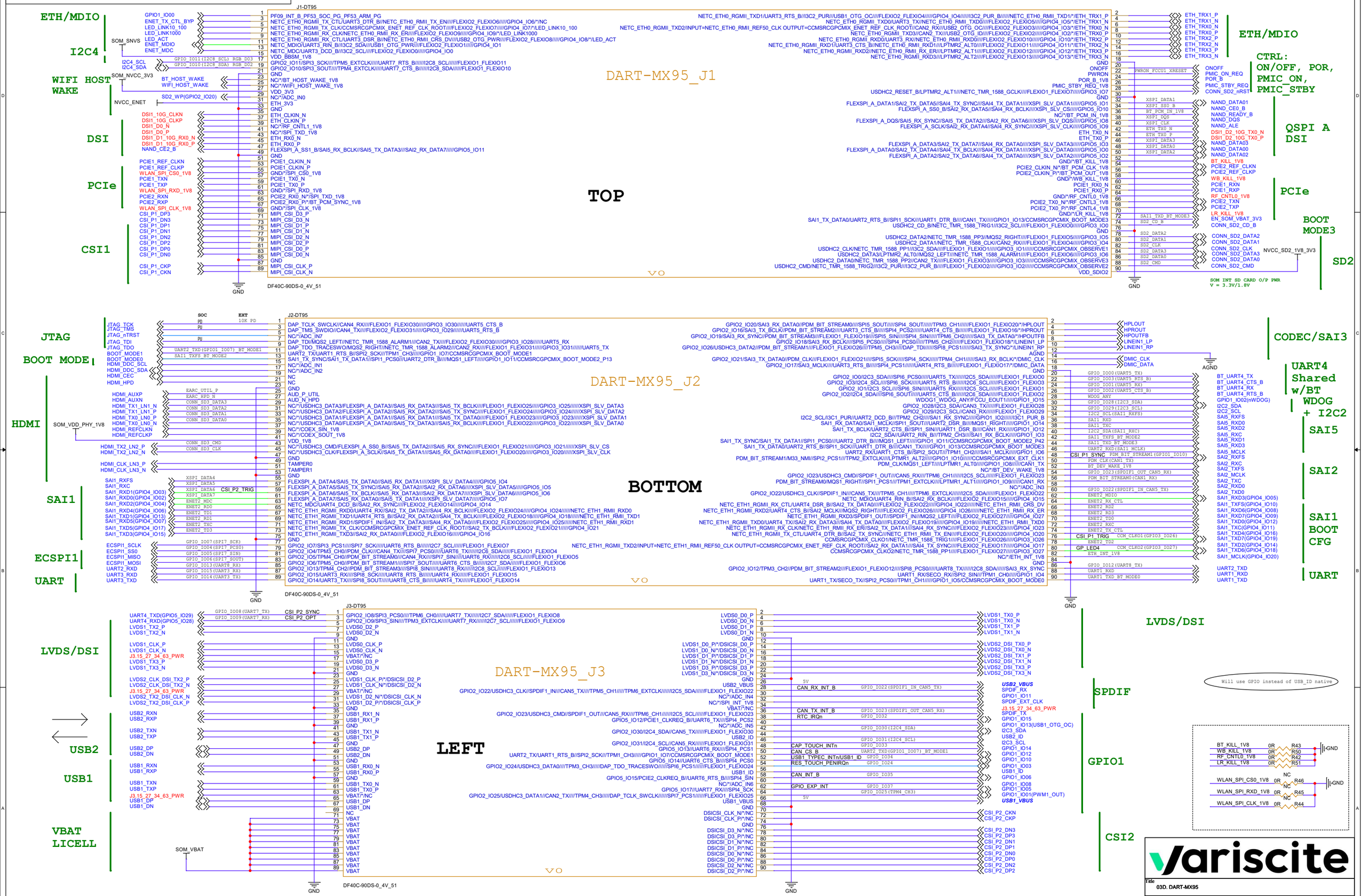


Note: Pinname with /*/ prefix denotes a HW assy option.

variscite

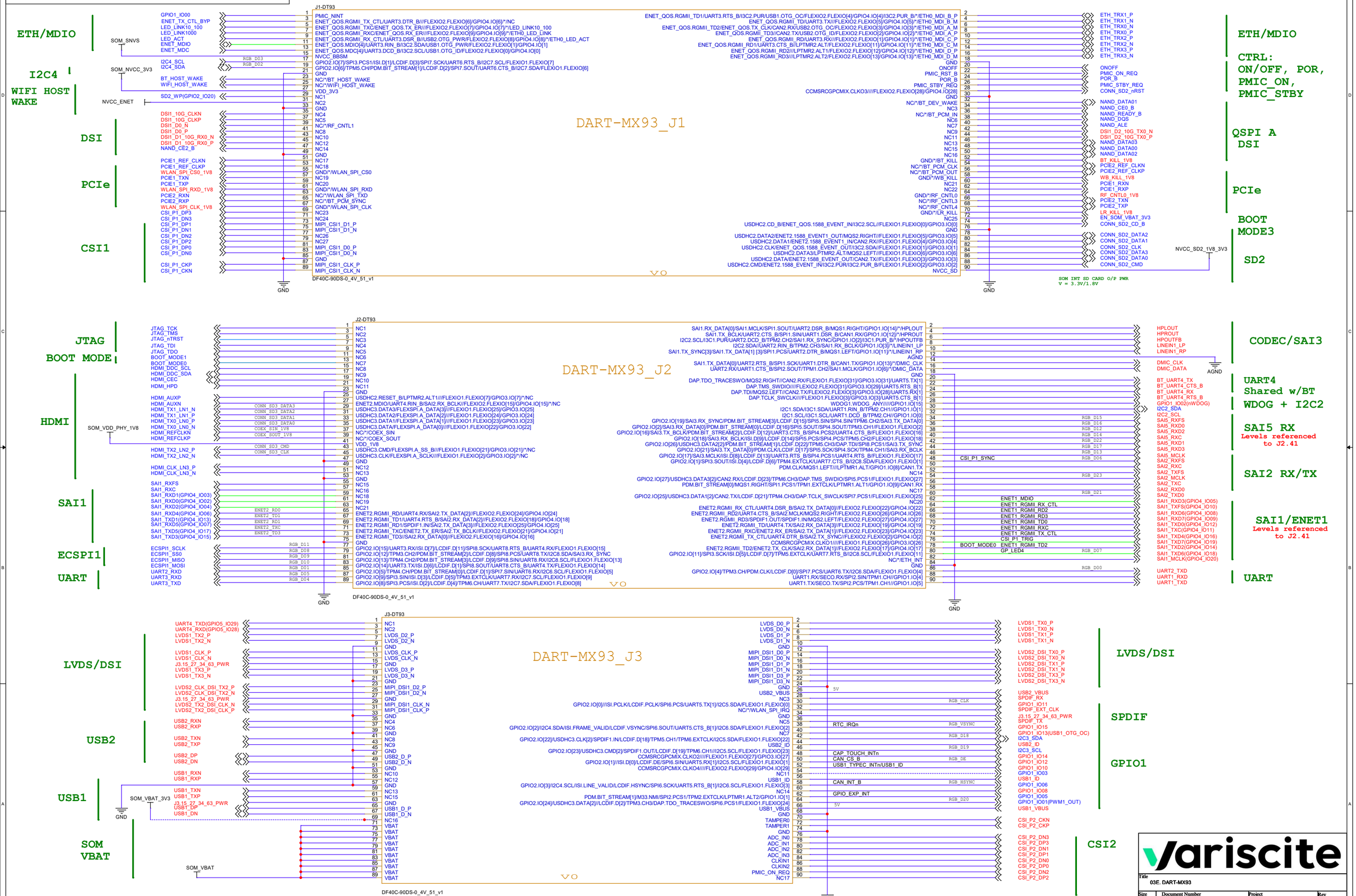
Title: 03C. DART-MX8M-PLUS			
Size: A2	Document Number: Sonata Board	Project: Sonata Board	Rev: R1.1C_D1.4
Designer: Shay V.		Approved By:	
Date: Sunday, October 05, 2025		Sheet 10 of 23	

03D - DART-MX95 Connectors

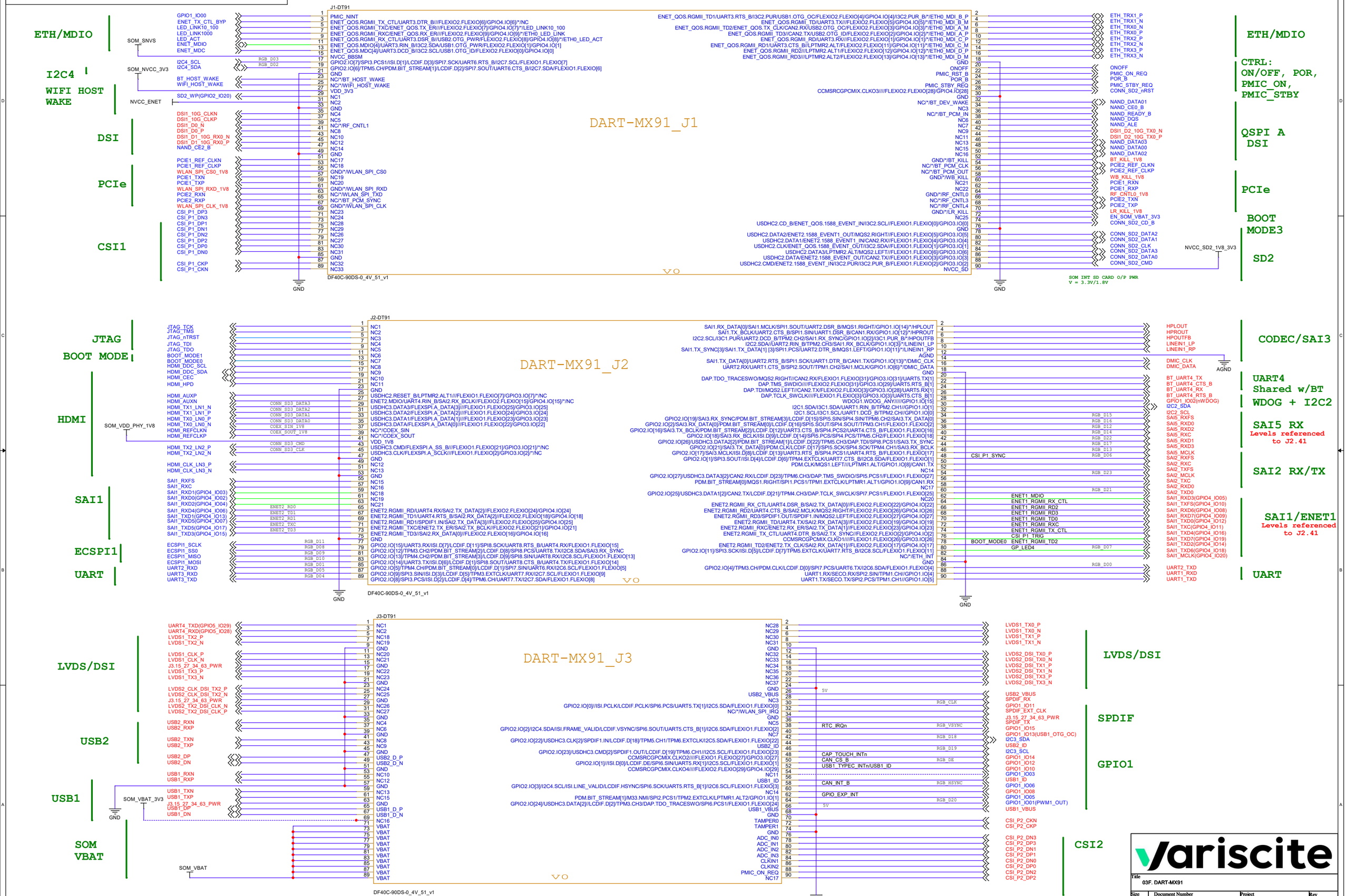


Title	03D. DART-MX95
Size	A2
Document Number	Sonata Board
Project	Sonata Board
Rev	R1.1C_D1.4
Designer:	Shay V.
Approved By:	
Date:	Sunday, October 05, 2025
Sheet	11 of 23

03E - DART-MX93 Connectors



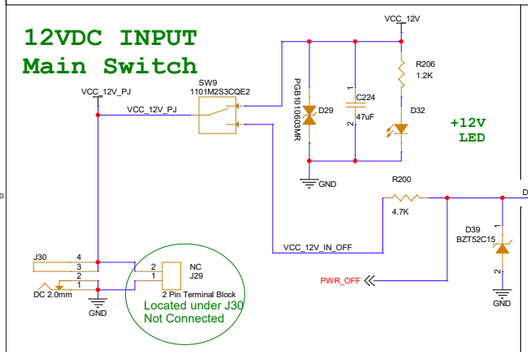
03F - DART-MX91 Connectors



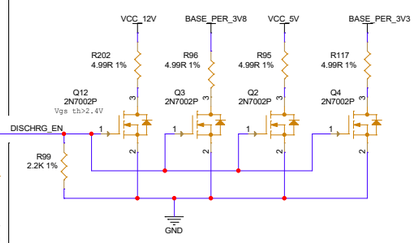
Title	03F. DART-MX91
Size	A2
Document Number	Sonata Board
Project	Sonata Board
Rev	R1.1C_D1.4
Designer:	Shay V.
Approved By:	
Date:	Sunday, October 05, 2025
Sheet	13 of 23

04. Power, RTC,Board ID

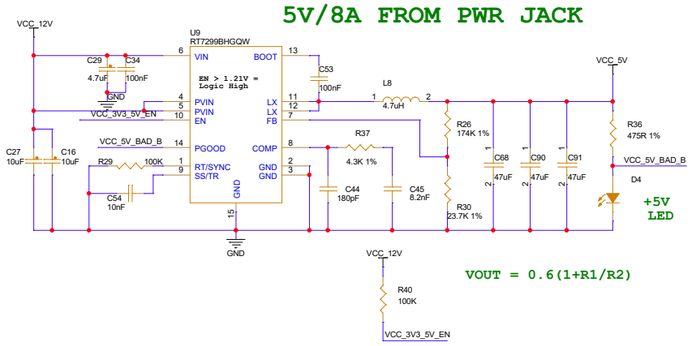
12VDC INPUT Main Switch



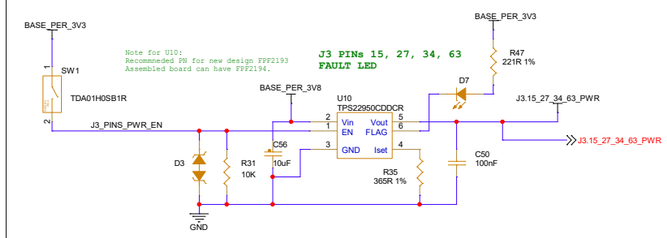
POWER DISCHARGE



5V/8A FROM PWR JACK

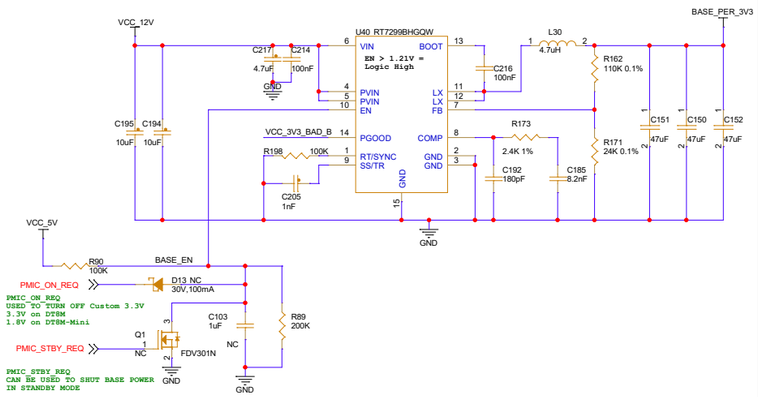


J3 PINS 15 27 34 63 POWER

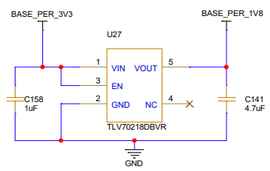


Switch deafults to OFF,
Must be set to ON when connecting
DT95 SOM

3.35V/8A FROM PWR JACK

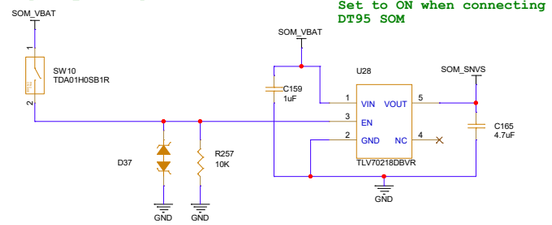


1.8V/0.3A BASE

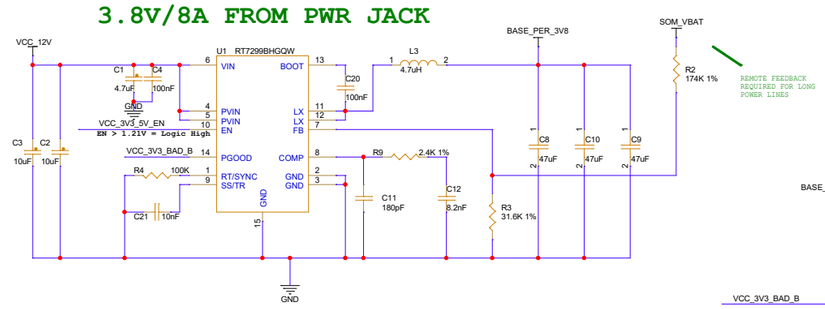


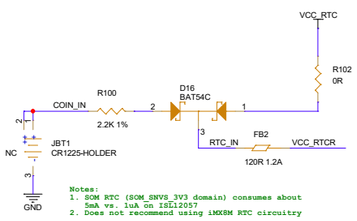
Workaround for NXP DART-MX95 bring up bug

Switch deafults to OFF,
Set to ON when connecting
DT95 SOM

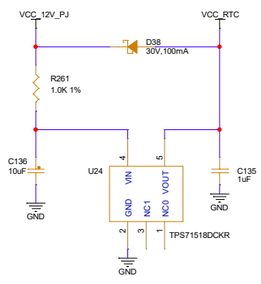


3.8V/8A FROM PWR JACK

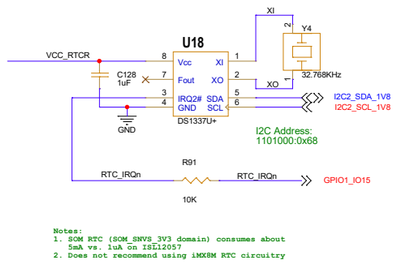




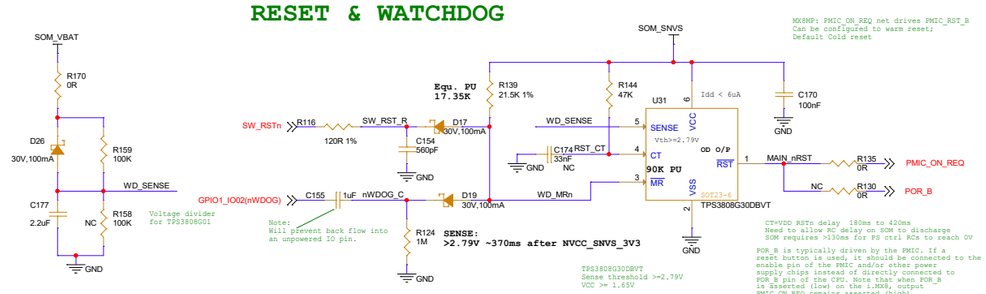
RTC LDO Option



RTC BATTERY

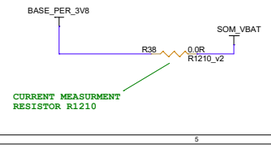


RESET & WATCHDOG

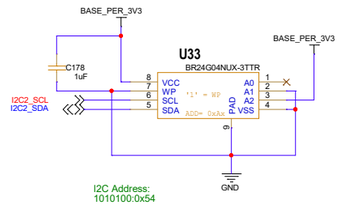


SOM SNVS

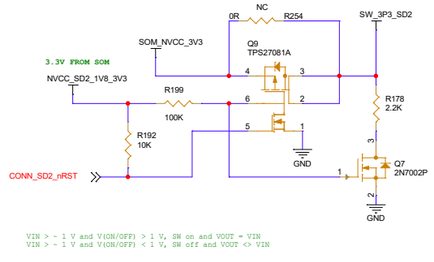
SOM PWR



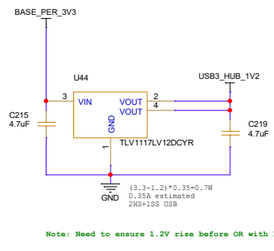
BOARD ID



SD POWER

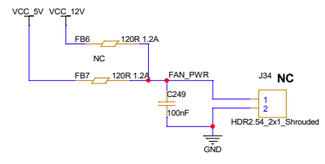


USB3 HUB POWER



Note: Need to ensure 1.2V rise before OR with 3.3V

FAN : 5V/0.2A



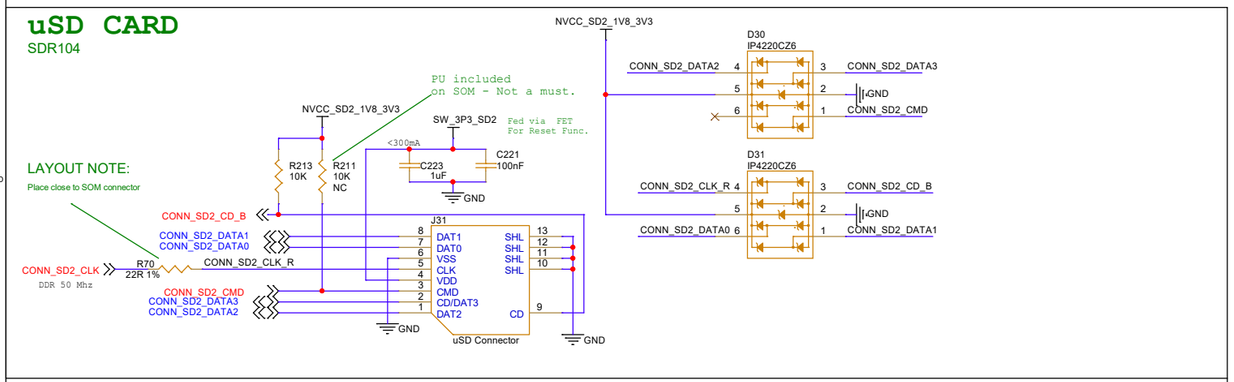
variscite

Title	04. Power, RTC, BoardID
Size: Custom	Document Number: Sonata Board
Project: Sonata Board	Rev: R1.1C_D1.4
Designer: Shay V.	Approved By:
Date: Wednesday, November 26, 2025	Sheet 14 of 23

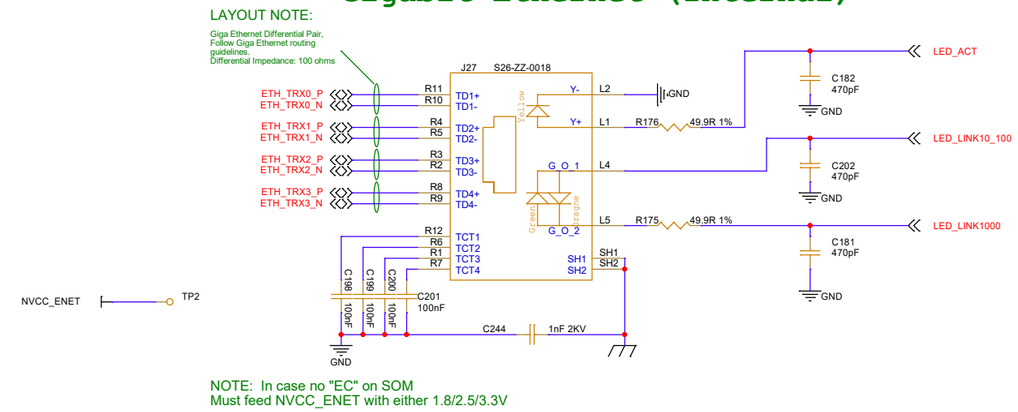
05. ETH, uSD, AUDIO, MIPI-CSI

uSD CARD

SDR104



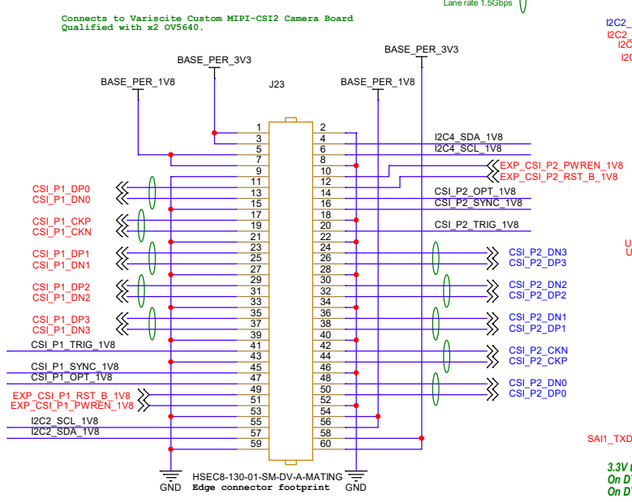
Gigabit Ethernet (Internal)



NOTE: In case no "EC" on SOM
Must feed NVCC_ENET with either 1.8/2.5/3.3V

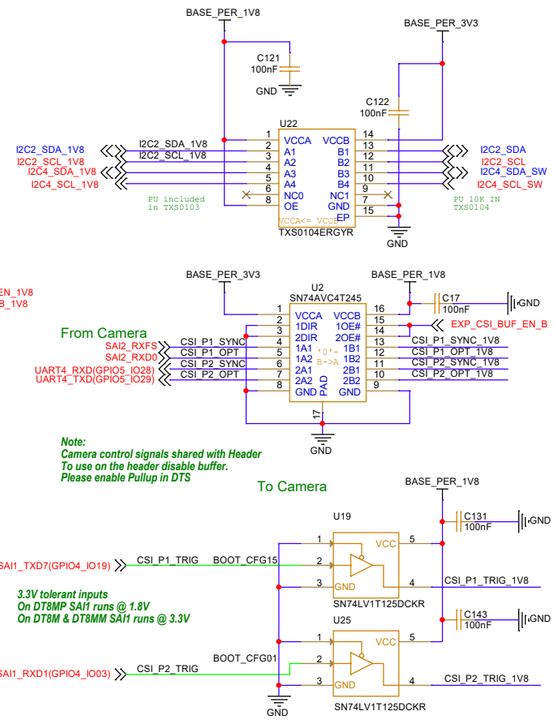
MIPI-CSI0 + MIPI-CSI1

Connects to Variscite Custom MIPI-CSI2 Camera Board
Qualified with x2 OV5640.



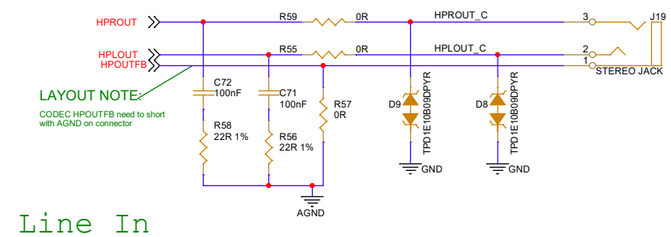
NOTE:

1. I2C and GPIO run @ 1.8V
2. Camera reference clock generated on camera board
3. SN74AVC4T245 DIR+OE ref'd to VccA

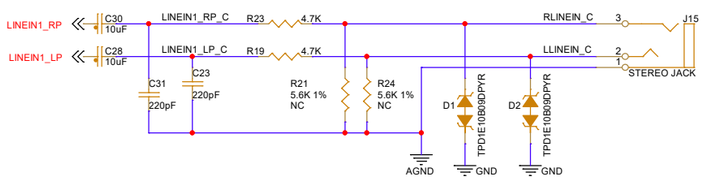


AUDIO

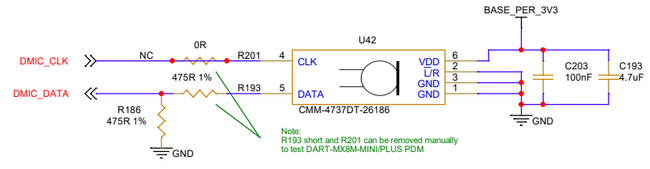
Headphones



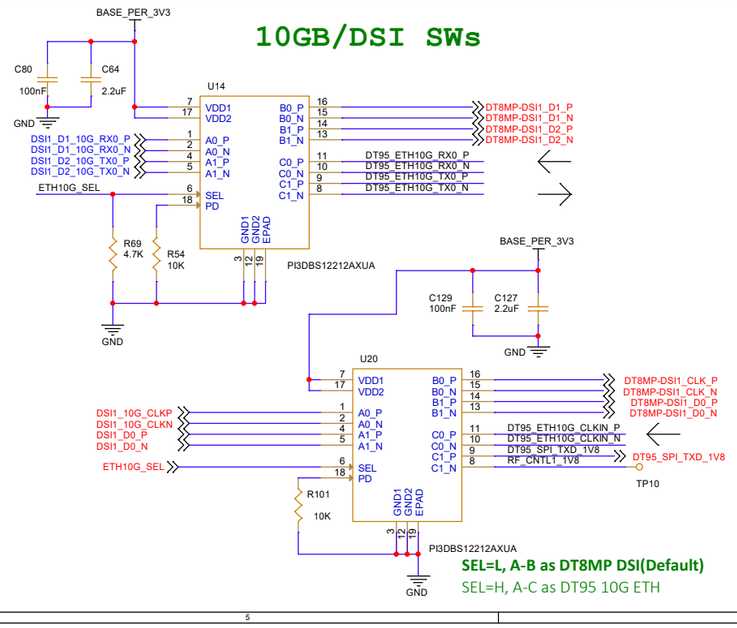
Line In



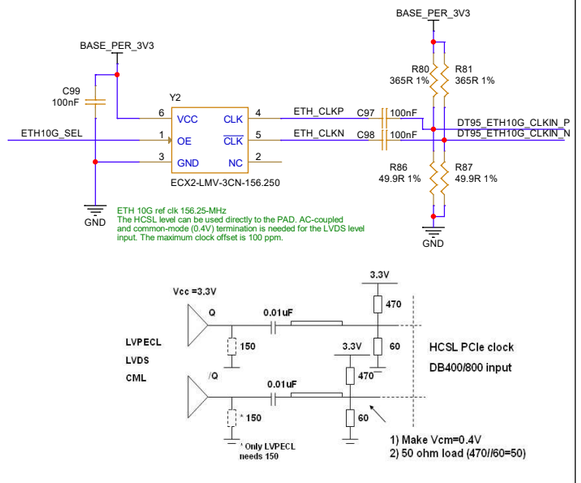
DIGITAL MIC



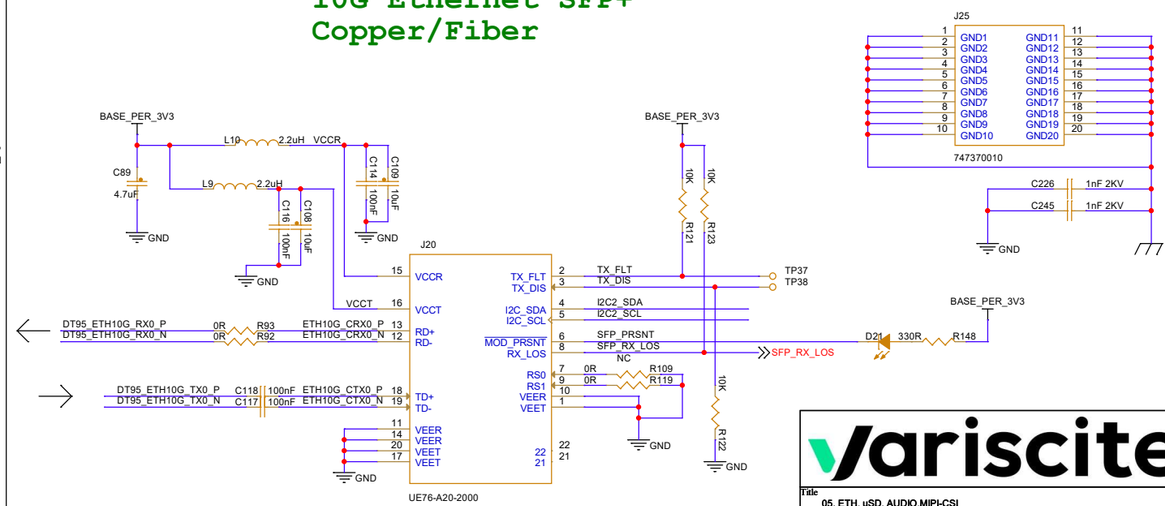
10GB/DSI SWs



ETH 10G ref clk 156.25MHz LVDS



10G Ethernet SFP+ Copper/Fiber

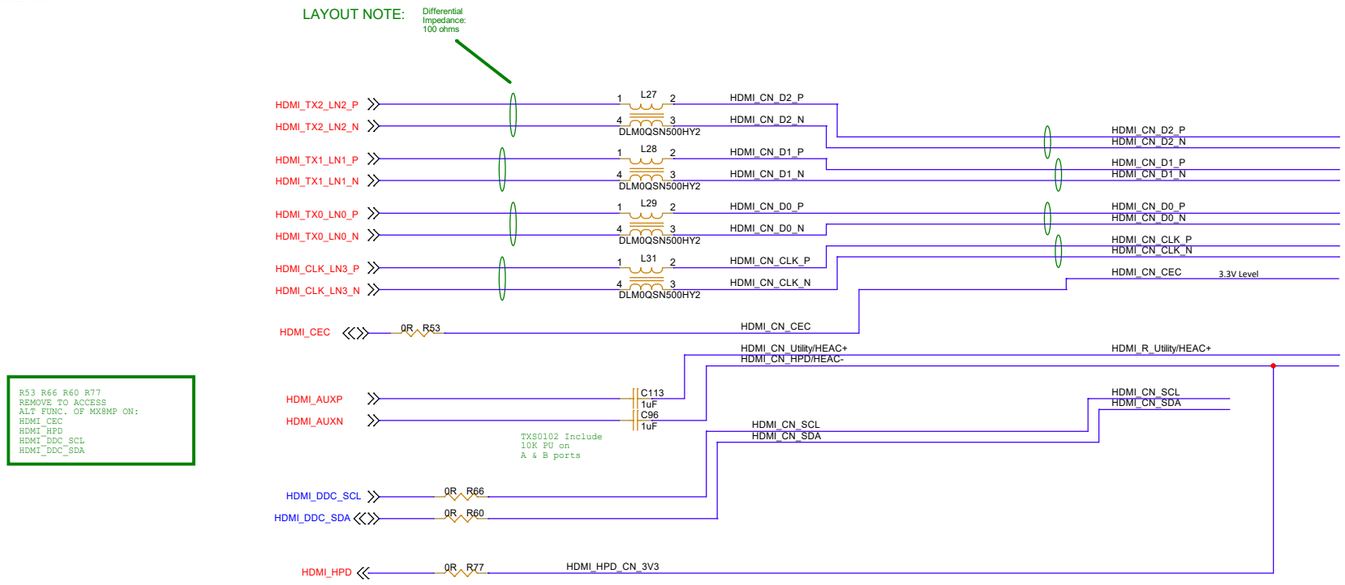


variscite

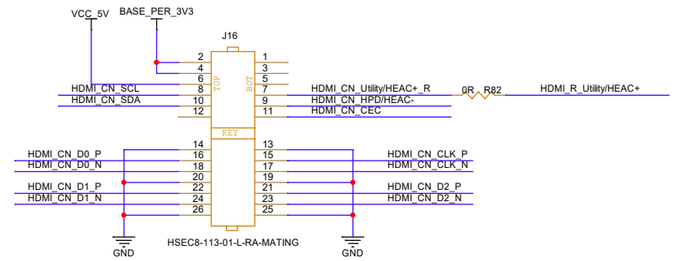
Title: 05. ETH, uSD, AUDIO,MIPI-CSI			
Size: A2	Document Number: Sonata Board	Project: Sonata Board	Rev: R1.1C_D1.4
Designer: Shay V		Approved By:	
Date: Wednesday, November 26, 2025		Sheet 15 of 23	

06. HDMI

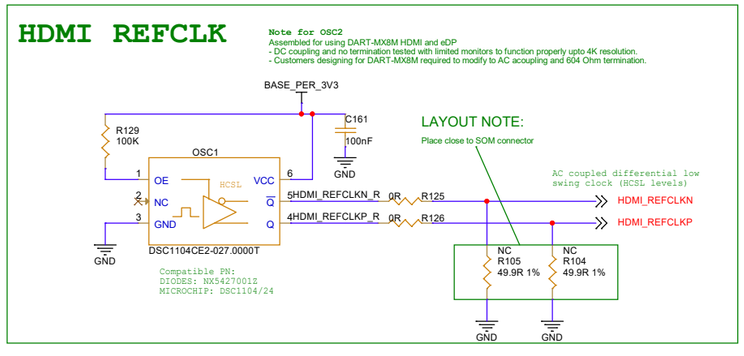
HDMI PATH



HDMI EDGE CONNECTOR



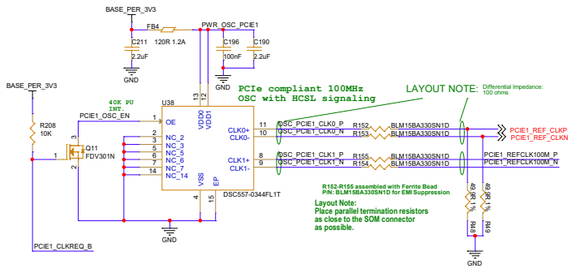
HDMI REFCLK



Title: 06. HDMI			
Size: A2	Document Number: Sonata Board	Project: Sonata Board	Rev: R1.1C_D1.4
Designer: Shay V		Approved By: <Approved By>	
Date: Sunday, October 05, 2025		Sheet 16 of 23	

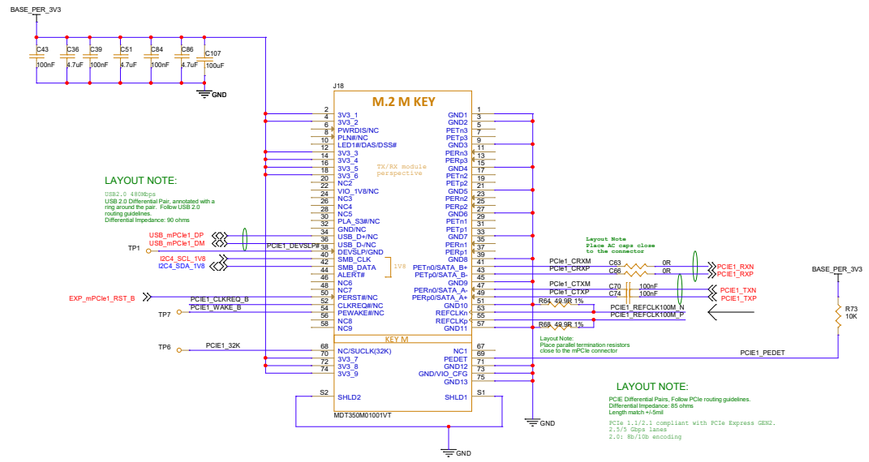
07. PCIe, QSPI, MIPI-DSI, USB DEBUG

PCIe1 CLK DIST.

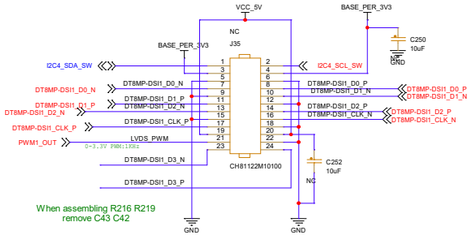


DART-MX8M Note:
The SOM won't complete boot process unless one of the following will be done:
1. PCI1 bus is disabled via software
2. PCI1 M.2 module is plugged
3. Q11 is removed

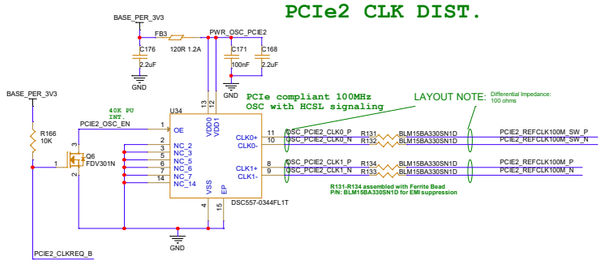
PCIe1 M.2 M Key Vertical Connector



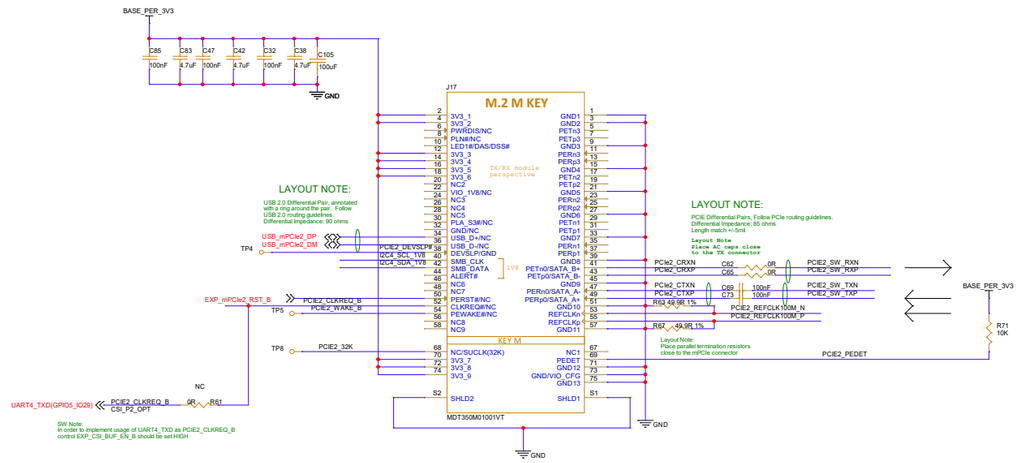
DART-MX8MP MIPI-DSI ON PS Compatible to Symphony J7+J8



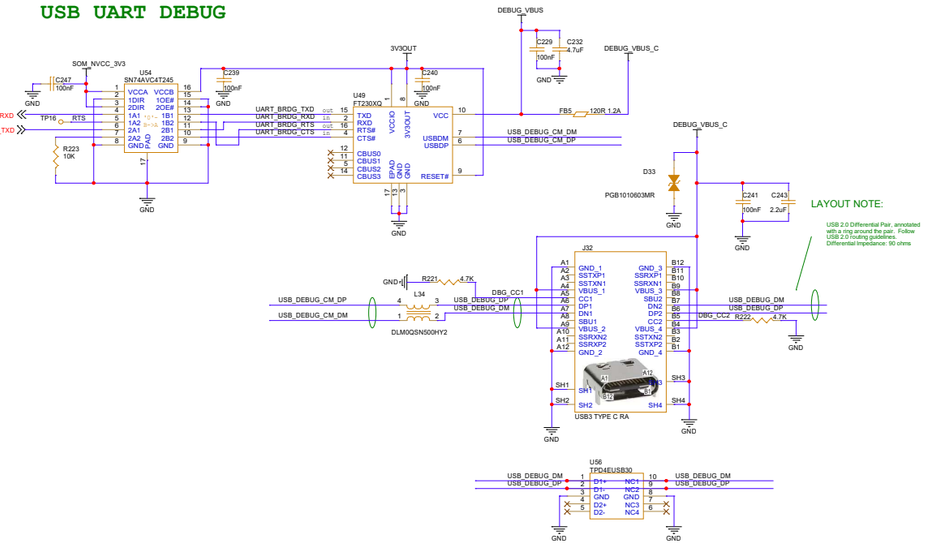
PCIe2 CLK DIST.



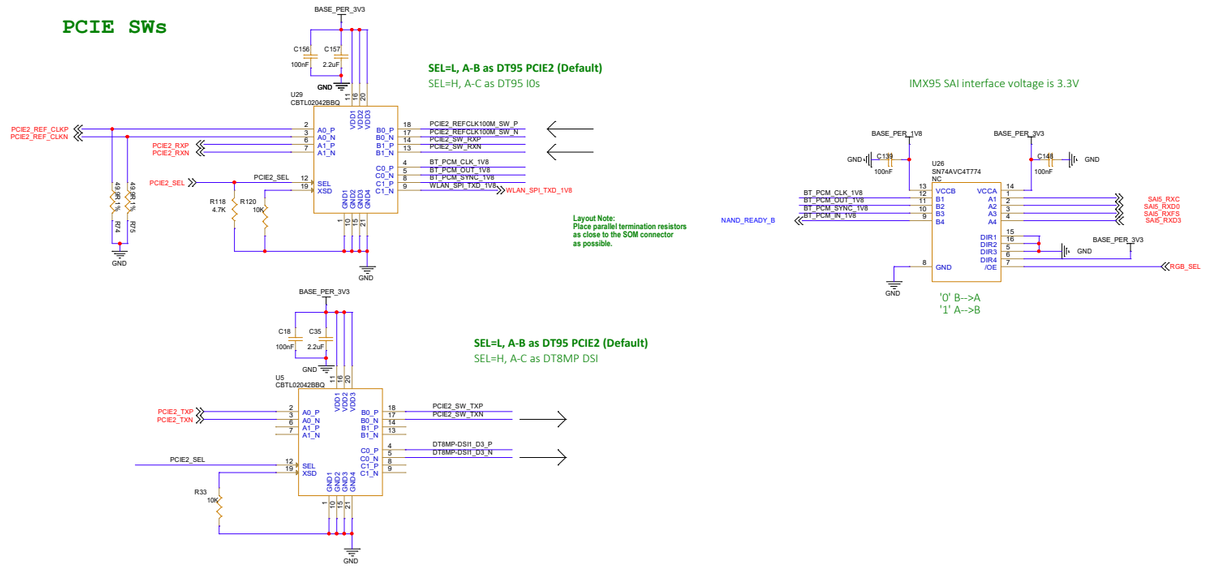
PCIe2 M.2 M Key Vertical Connector



USB UART DEBUG



PCIE SWs

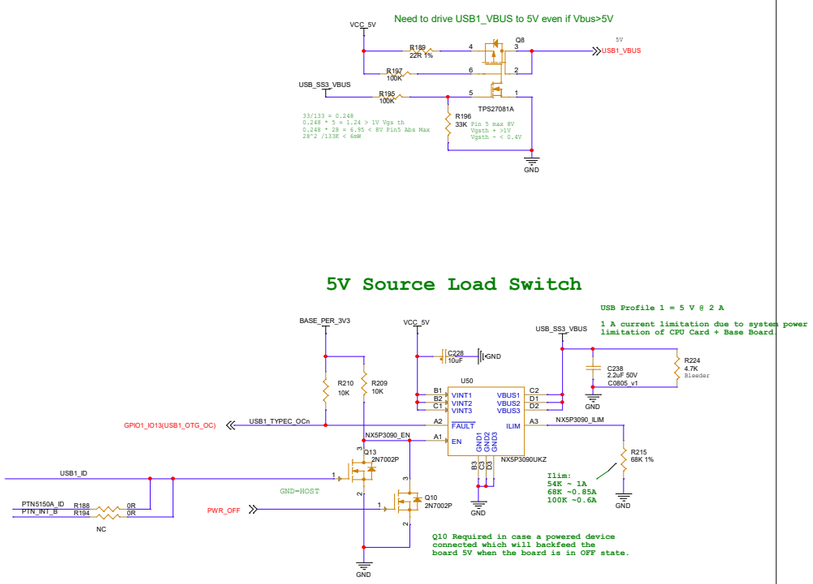


variscite

Title: 07. PCIe, MIPI-DSI,UART DBG			
Size: A1	Document Number: Sonata Board	Project: Sonata Board	Rev: R1.1C_D1.4
Designer: Shay V.		Approved By:	<Approved By>
Date: Tuesday, November 18, 2025		Sheet 17 of 23	

08. USB TYPE C, USB 3 HUB

USB#1 - DRP USB TYPE C

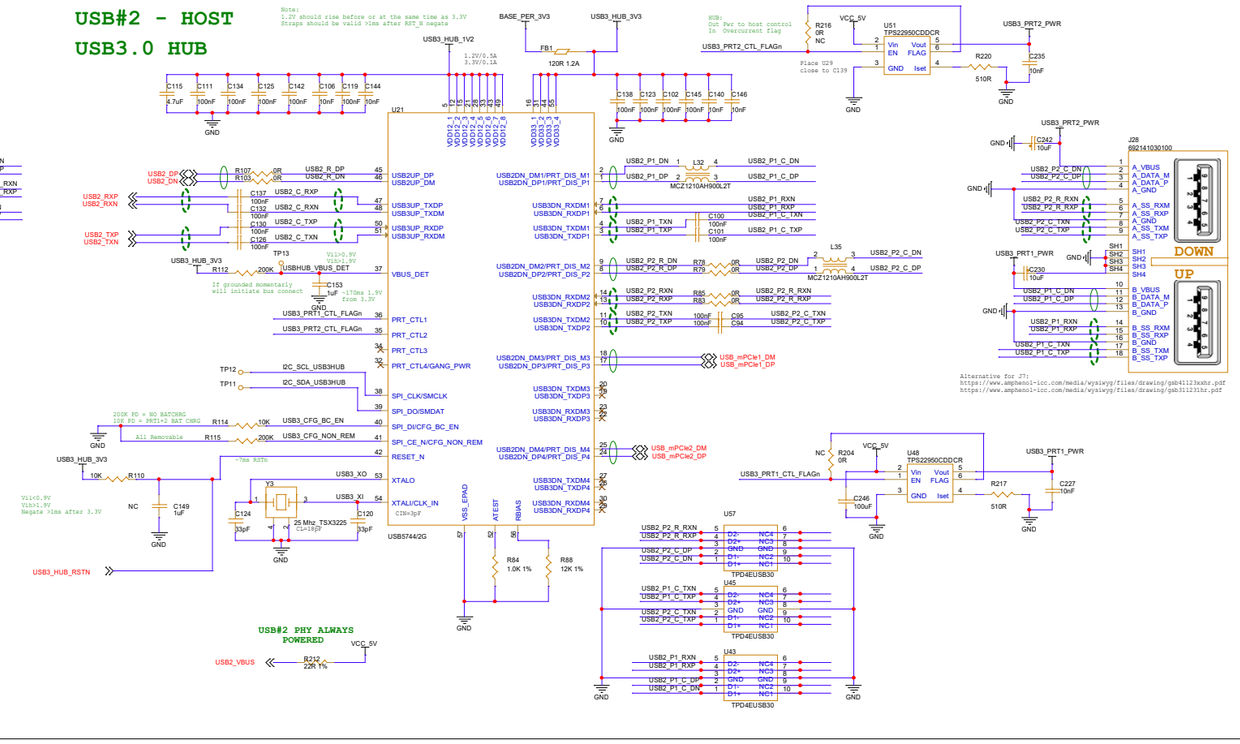


USB HUB Bypass to Port A Connector

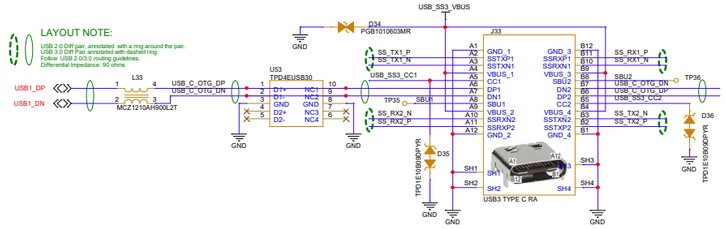
USB2_DN	NC	R238	0R	USB2_P2_BY_DN	NC	R230	0R	USB2_P2_DN			
USB2_DP	NC	R239	0R	USB2_P2_BY_DP	NC	R231	0R	USB2_P2_DP			
USB2_RXN	NC	R236	0R	USB2_P2_BY_RXN	NC	R232	0R	USB2_P2_R_RXN			
USB2_RXP	NC	R237	0R	USB2_P2_BY_RXP	NC	R233	0R	USB2_P2_R_RXP			
USB2_TXN	NC	R234	0R	USB2_P2_BY_TXN	NC	100nF	C256	USB2_P2_C_TXN			
USB2_TXP	NC	R235	0R	USB2_P2_BY_TXP	NC	100nF	C257	USB2_P2_C_TXP			

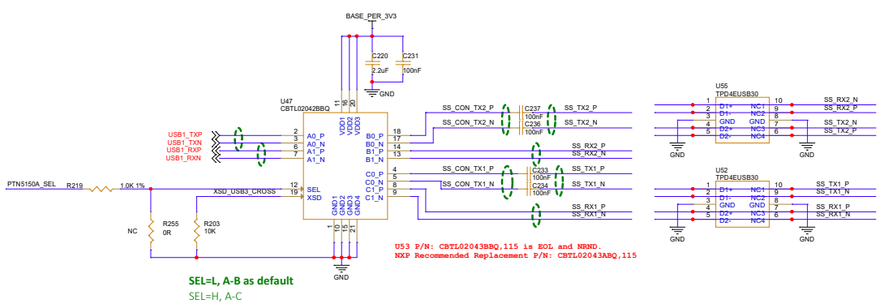
Put 0 PS	Put 0 PS
R239 under R107	R230 under R78
R238 under R103	R231 under R79
R237 under C137	R232 under R85
R236 under C132	R233 under R83
R235 under C130	C256 under C95
R234 under C126	C257 under C94

USB#2 - HOST USB3.0 HUB

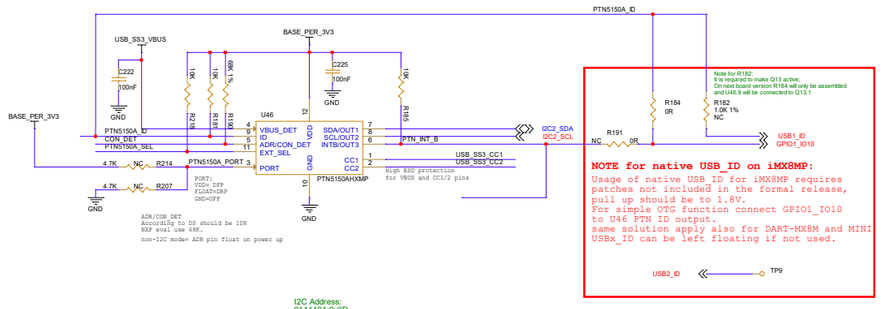


USB3.0 Type-C crossbar switch





Config Channel Logic Detection & Indication of Plug Orientation



I2C Address:
0111101:0x3D

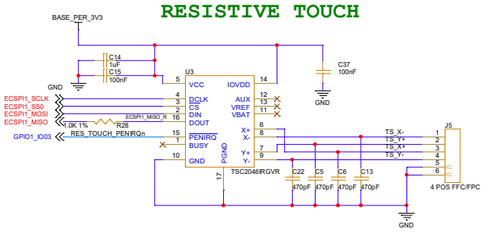
Note:
VBUS active discharge replaced with bleeder

variscite

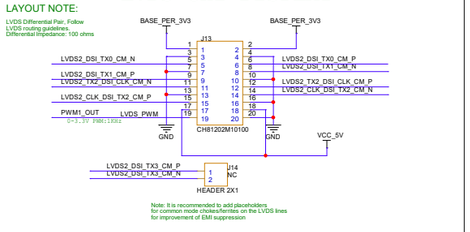
Title: 08. USB C OTG, USB HOST			
Size: A1	Document Number: Sonata Board	Project: Sonata Board	Rev: R1.1C_D1.4
Designer: Shay V.		Approved By:	
Date: Sunday, October 05, 2025		Sheet 18 of 23	

09. LVDS, TOUCH, JTAG, I2C EXP

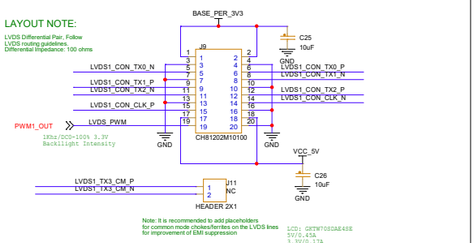
RESISTIVE TOUCH



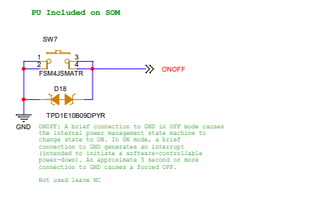
LVDS CH1 DISPLAY



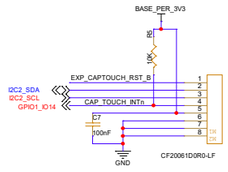
LVDS DISPLAY CH0



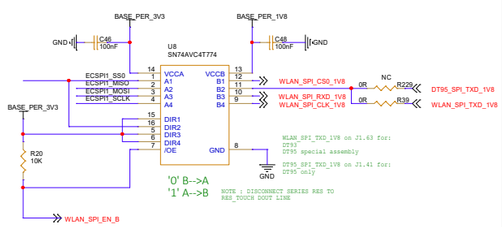
ON/OFF



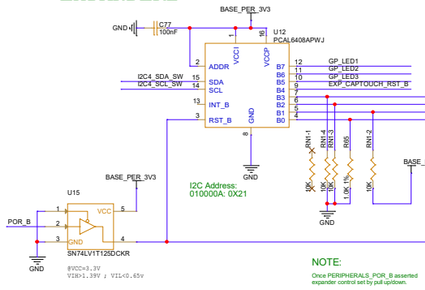
CAPACITIVE TOUCH



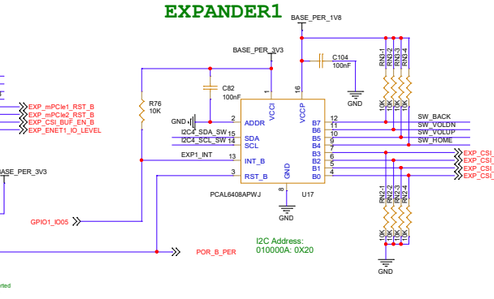
SPI BUFFER for WBE



GPIO EXPANDER2

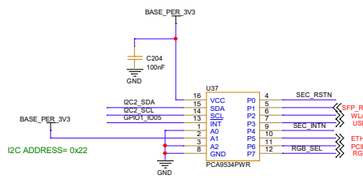


GPIO EXPANDER1

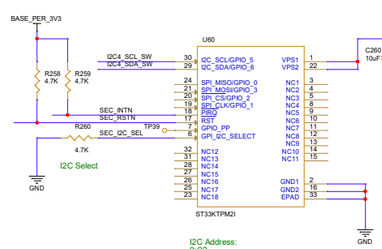


NOTE:
Once PERIPHERALS_POR_B asserted
expander control set by pull up/down.

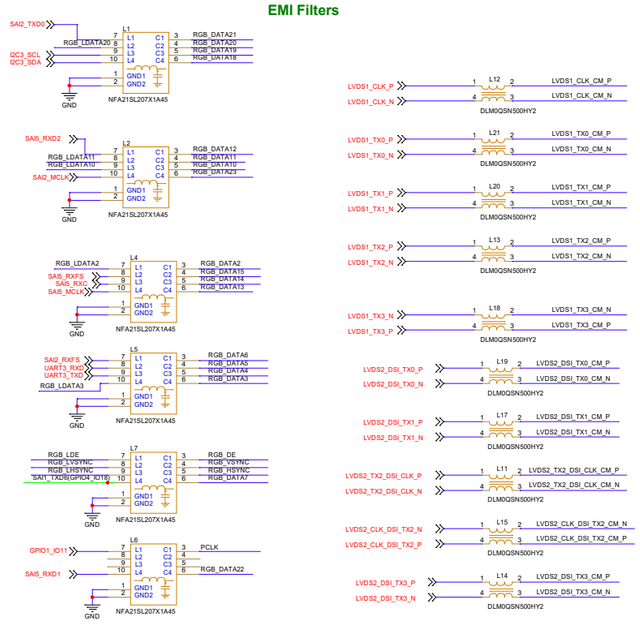
GPIO EXPANDER3



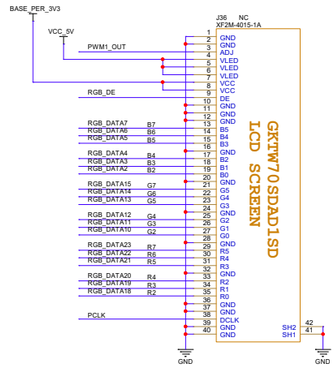
Trusted Platform Module (TPM)



EMI Filters

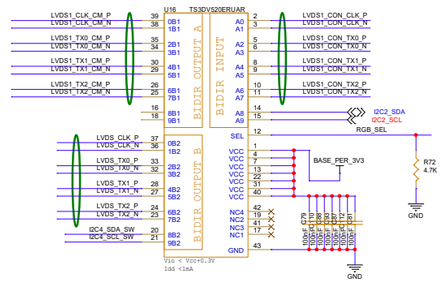


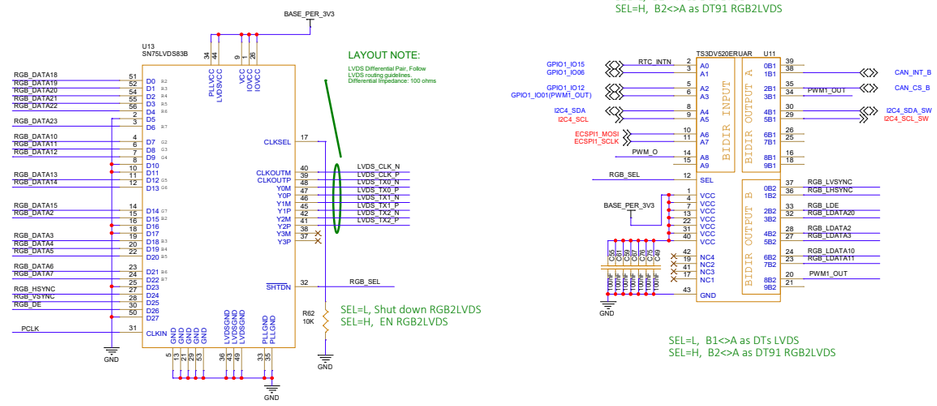
RGB 666 LCD



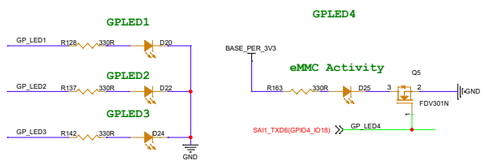
Parallel RGB 666 to LVDS Bridge DT91
24-Bit Color Host to 18-Bit Color LCD

LVDS SWs



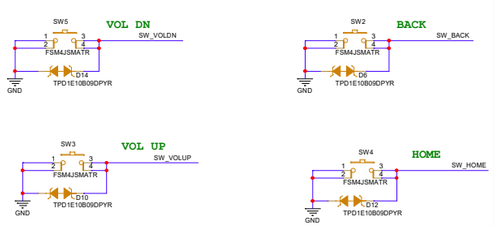


GP LEDS

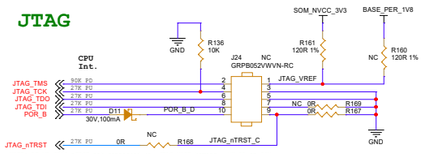


RST

GP BUTTONS



JTAG



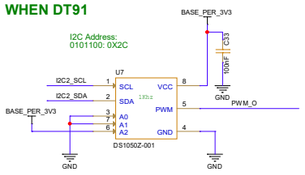
The new 10 pin smaller connector is now becoming an industry standard.

The ARM DStream comes with a 10-pin connector. If you need a ribbon, they can be purchased at Digikey:
Samtec Inc MPN: FFSD-05-D-04.00-01-N

If you need to expand to a 20-pin connector for a different JTAG device, the expander board can also be purchased at Digikey:
Olimex LTD MPN: ARM-JTAG-20-10

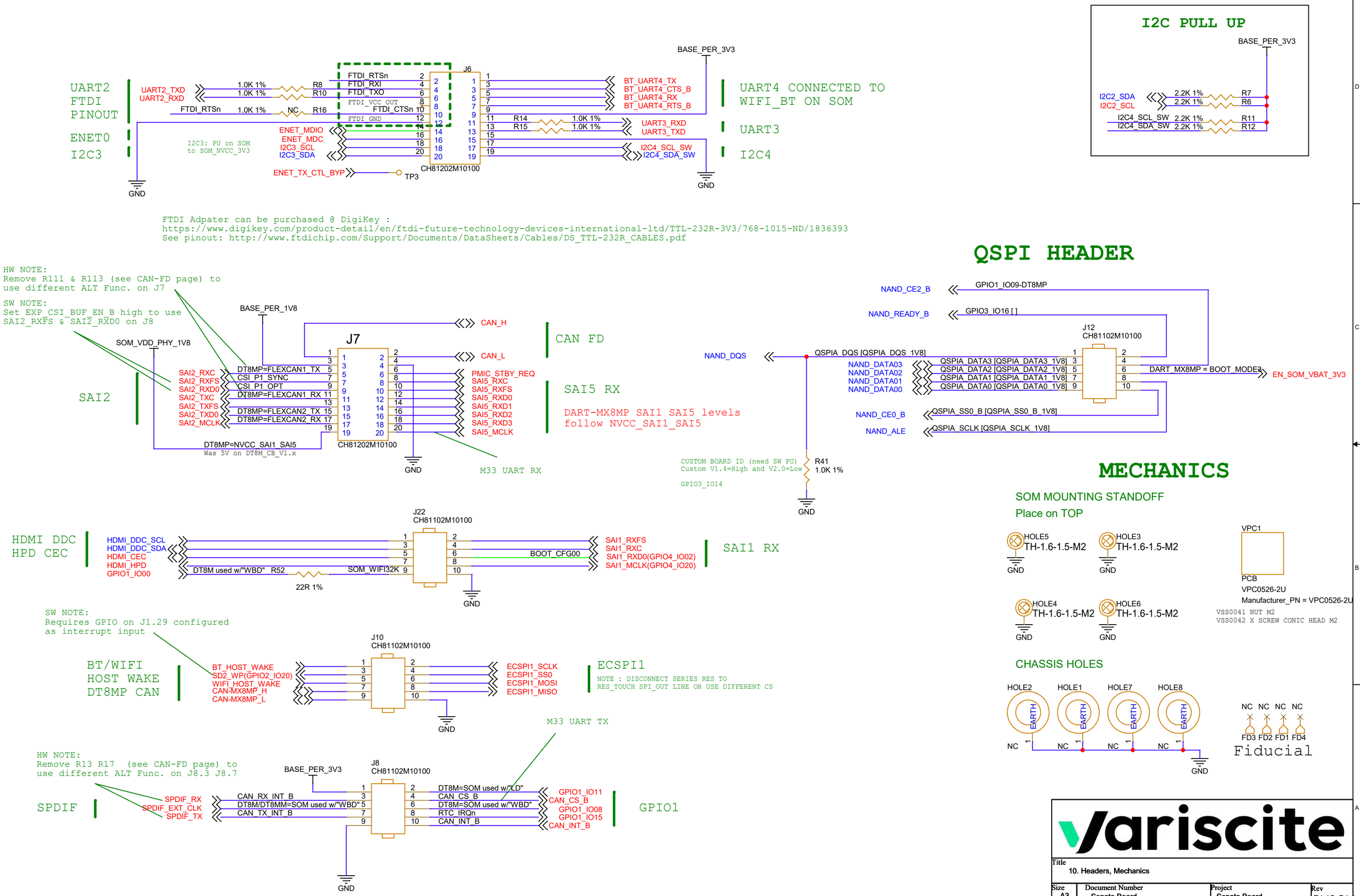
https://www.digikey.com/products/en/development-boards-kits-programmers/accessories/783?k=JTAG%20adapter

PWM WHEN DT91



Title	09. LCD, JTAG, I2C EXP,GPIO,SEC
Size A1	Document Number Sonata Board
Project Sonata Board	Rev R1.1C_D1.4
Designer: Shay V	Approved By:
Date: Sunday, October 05, 2025	Sheet 19 of 23

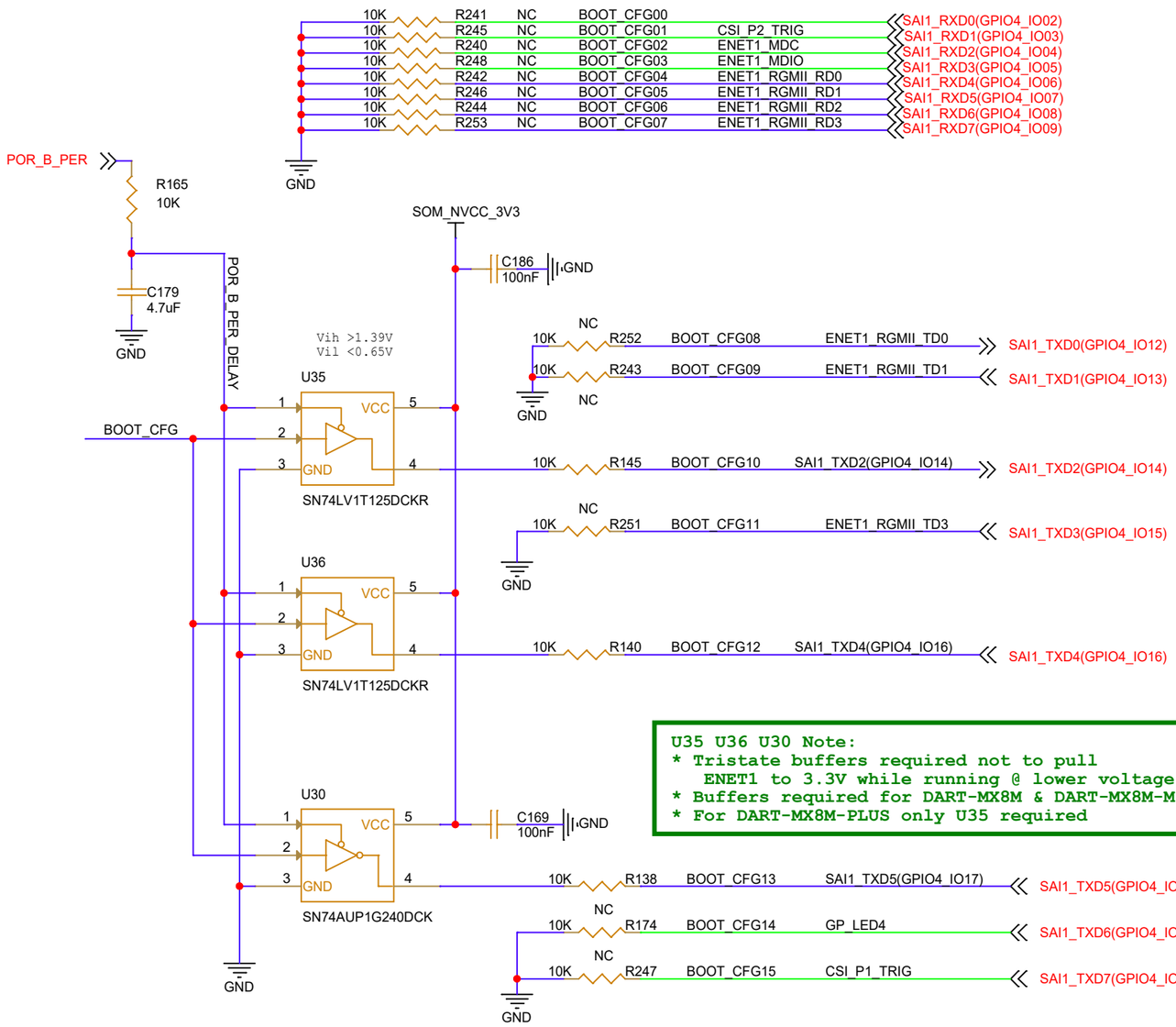
10. HEADERS, Mechanics, Pull Ups



Title: 10. Headers, Mechanics			
Size: A3	Document Number: Sonata Board	Project: Sonata Board	Rev: R1.1C_D1.4
Designer: Shay V.		Approved By:	
Date: Sunday, October 05, 2025		Sheet 20 of 23	

11. BOOT CONFIG & MODE

			INT. BOOT	EXT. BOOT	
SAI1_RXD0(GPIO4_IO02)		BOOT_CFG00	0	0	Need to Enable PU in DTS; See pp. 5
SAI1_RXD1(GPIO4_IO03)	CSI_P2_TRIG	BOOT_CFG01	0	0	
SAI1_RXD2(GPIO4_IO04)	ENET1_MDC	BOOT_CFG02	0	0	
SAI1_RXD3(GPIO4_IO05)	ENET1_MDIO	BOOT_CFG03	0	0	
SAI1_RXD4(GPIO4_IO06)	ENET1_RGMII_RD0	BOOT_CFG04	0	0	
SAI1_RXD5(GPIO4_IO07)	ENET1_RGMII_RD1	BOOT_CFG05	0	0	
SAI1_RXD6(GPIO4_IO08)	ENET1_RGMII_RD2	BOOT_CFG06	0	0	
SAI1_RXD7(GPIO4_IO09)	ENET1_RGMII_RD3	BOOT_CFG07	0	0	
SAI1_TXD0(GPIO4_IO12)	ENET1_RGMII_TD0	BOOT_CFG08	0	0	
SAI1_TXD1(GPIO4_IO13)	ENET1_RGMII_TD1	BOOT_CFG09	0	0	
SAI1_TXD2(GPIO4_IO14)	ENET1_RGMII_TD2	BOOT_CFG10	0	1	
SAI1_TXD3(GPIO4_IO15)	ENET1_RGMII_TD3	BOOT_CFG11	0	0	
SAI1_TXD4(GPIO4_IO16)	ENET1_RGMII_TX_CTL	BOOT_CFG12	0	1	
SAI1_TXD5(GPIO4_IO17)	ENET1_RGMII_TXC	BOOT_CFG13	1	0	
SAI1_TXD6(GPIO4_IO18)	GP_LED4	BOOT_CFG14	0	0	
SAI1_TXD7(GPIO4_IO19)	CSI_P1_TRIG	BOOT_CFG15	0	0	



U35 U36 U30 Note:
* Tristate buffers required not to pull ENET1 to 3.3V while running @ lower voltage.
* Buffers required for DART-MX8M & DART-MX8M-MINI
* For DART-MX8M-PLUS only U35 required

Notes:
a. Sampled on rising edge of POR_B
b. SOC PD during POR_B and after on BOOT CFG[15:0] and BOOTMODE[1:0]
c. BOOT_MODE[1:0] ="10" is Internal Boot - Always used.
d. Active boot cfg for one dip sw sel EXTERNAL/INTERNAL

DART-MX8M-MINI Notes:
b. Boot config lines do not follow the Mini datasheet in full DART-MX8M-MINI have added logic to be compatible to DART-MX8M

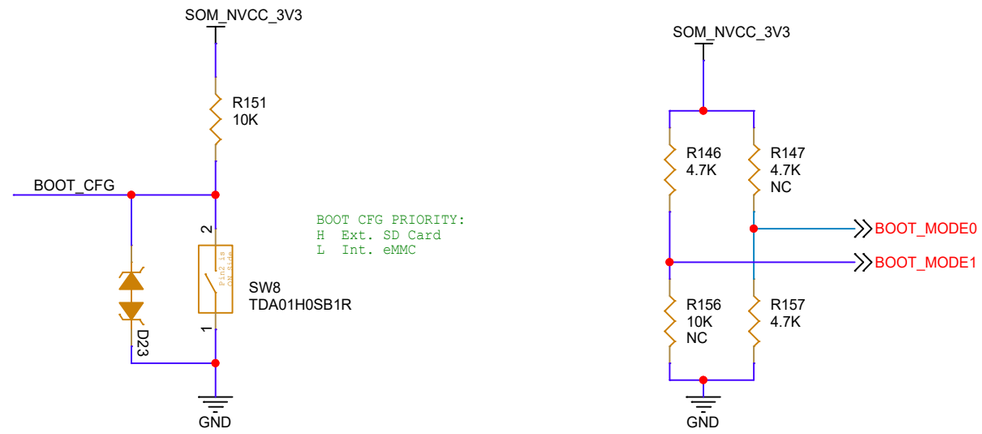
DART-MX8M-PLUS Notes:
a. Boot configuration set only by SAI1_TXD2 connected on DART via buffer to BOOT_MODE0

i.MX8M Plus Boot Mode

BOOT_MODE3	BOOT_MODE2	BOOT_MODE1	BOOT_MODE0	Boot Modes
0	0	0	0	Boot From Internal Fuses
0	0	0	1	USB Serial Download
0	0	1	0	USDHC3 (eMMC boot only, SD3 8-bit) Default
0	0	1	1	USDHC2 (SD boot only, SD2)

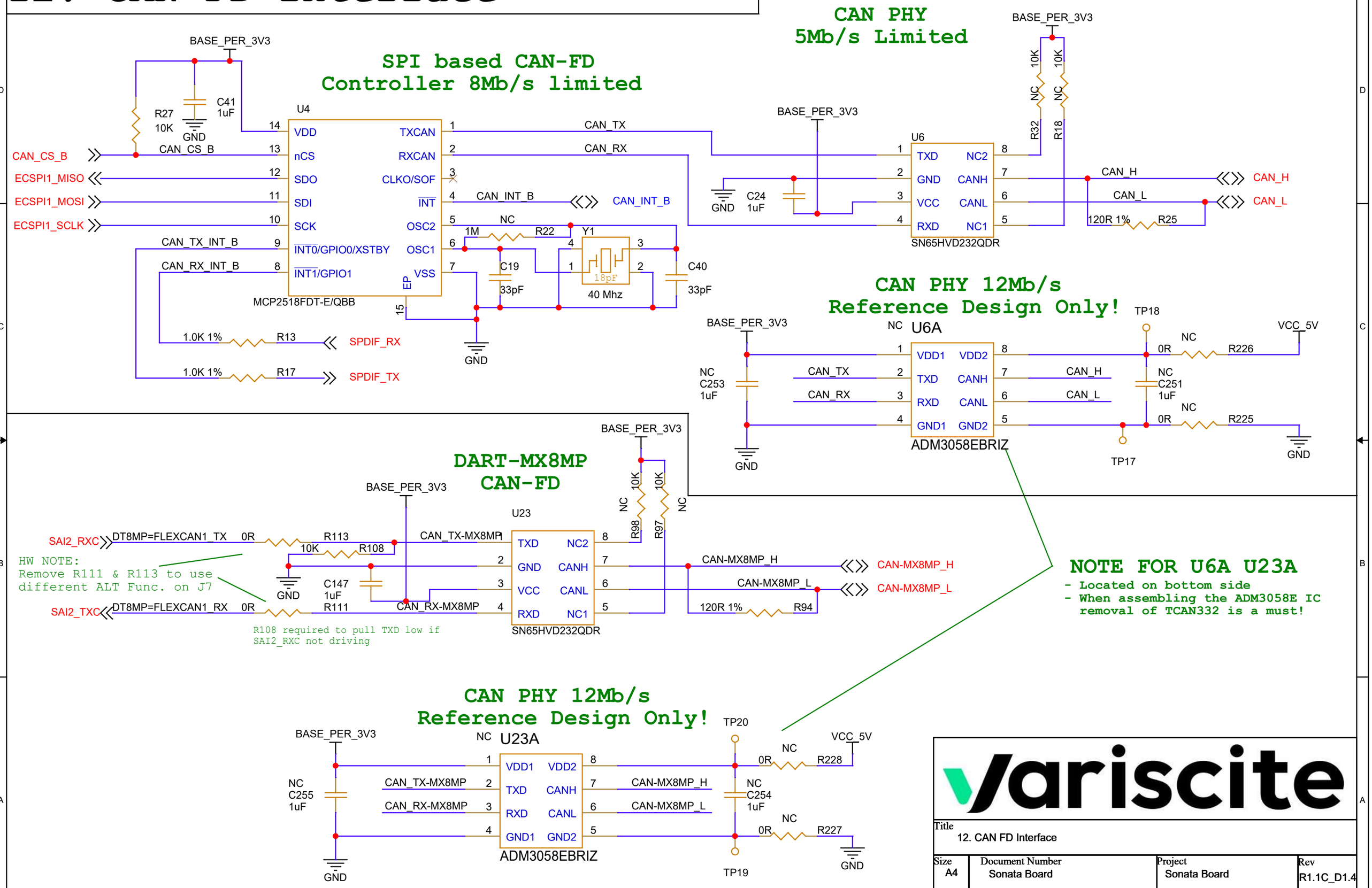
CustomBoard Net: BOOT_MODE0 SAI1_TXD2 EN_SOM_VBAT_3V3 BOOT_MODE1

DART-MX8MP BOOT MODE



Title: 11. BOOT CONFIG & MODE			
Size: B	Document Number: Sonata Board	Project: Sonata Board	Rev: R1.1C_D1.4
Designer: Shay V.		Approved By:	
Date: Sunday, October 05, 2025		Sheet 21 of 23	

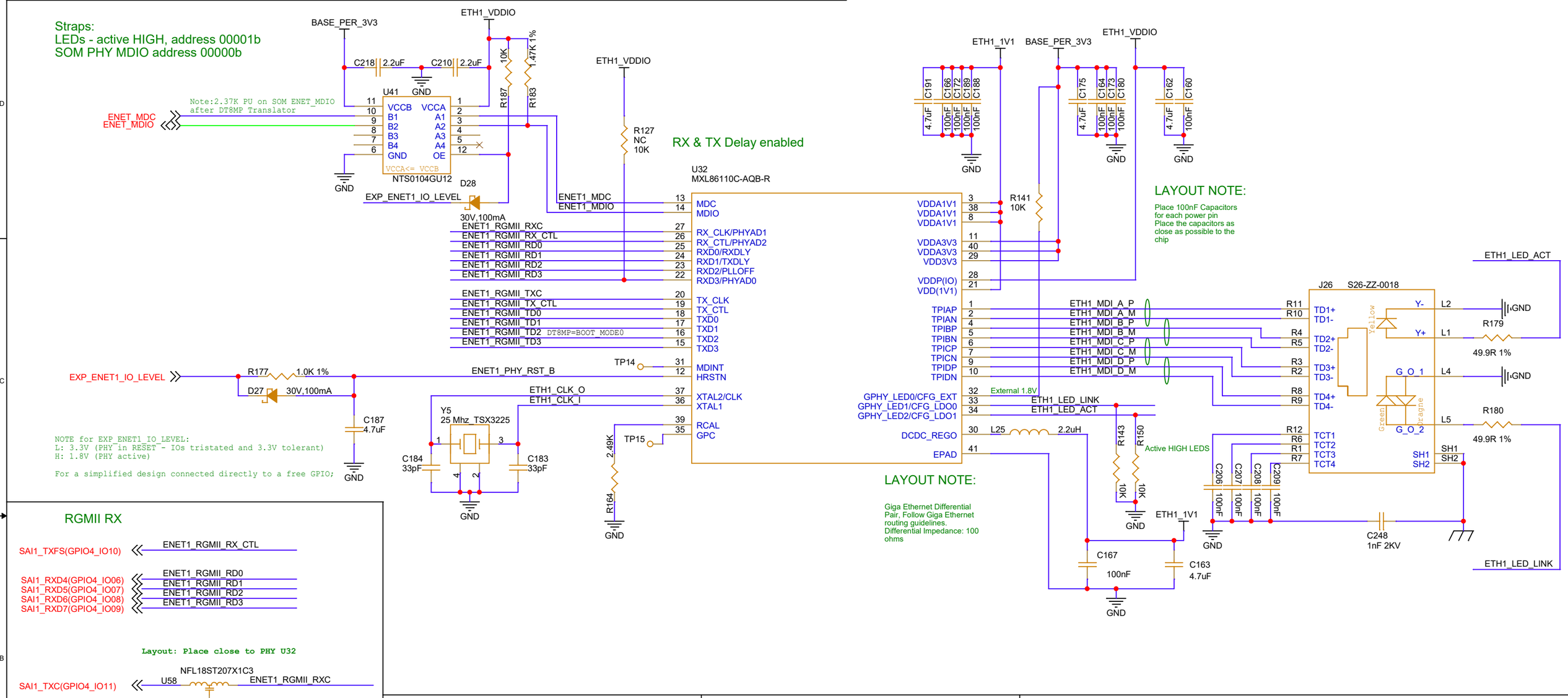
12. CAN FD Interface



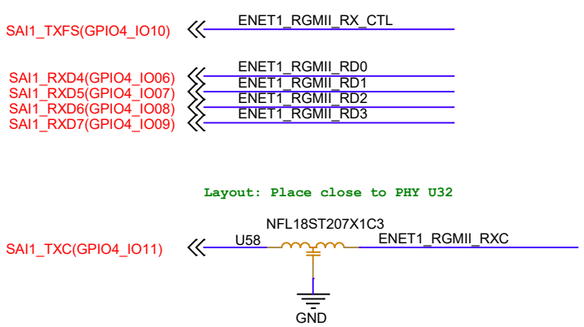
Title: 12. CAN FD Interface			
Size: A4	Document Number: Sonata Board	Project: Sonata Board	Rev: R1.1C_D1.4
Designer: Shay V.		Approved By:	
Date: Sunday, October 05, 2025		Sheet 22 of 23	

13. ENET1 Gigabit Ethernet

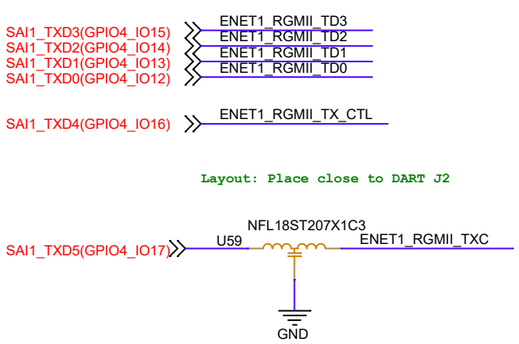
Straps:
LEDs - active HIGH, address 00001b
SOM PHY MDIO address 00000b



RGMII RX



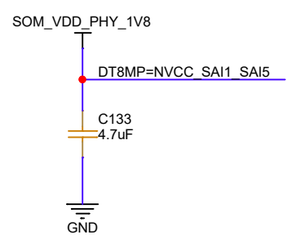
RGMII TX



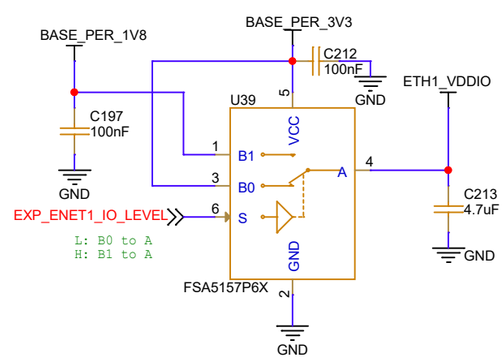
NOTE:
For DT8MP net SOM_VDD_PHY_1V8 connected to NVCC_SAI1_SAI5 which is an output from the DT8MPprogrammable PMIC LDO.

This output voltage will set SAI1 and SAI5 pads voltage level;
With DT8MCustomBoard-V1.x and earlier it is set to 3.3V. On DT8MCustomBoard-V2.x it is set to 1.8V for RGMII.

Bypass with 4.7uF min. 6.3V capacitor.

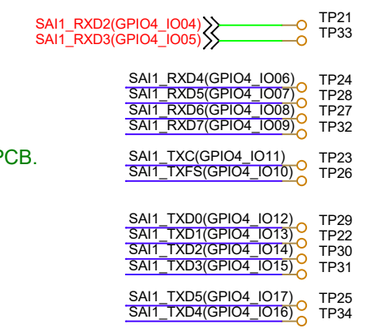


NOTE for U63:
Required for compatibility to DT8M & DT8MM where SAI1 levels are fixed to 3.3V;



NOTE:
Test points used to access DT8M & DT8MM SAI1 signals;

Levels are fixed to 3.3V by modules;
These test points located on the Print Side of the PCB.



Title: 13. Ethernet2			
Size: A3	Document Number: Sonata Board	Project: Sonata Board	Rev: R1.1C_D1.4
Designer: Shay V.		Approved By:	
Date: Wednesday, October 15, 2025		Sheet 23 of 23	