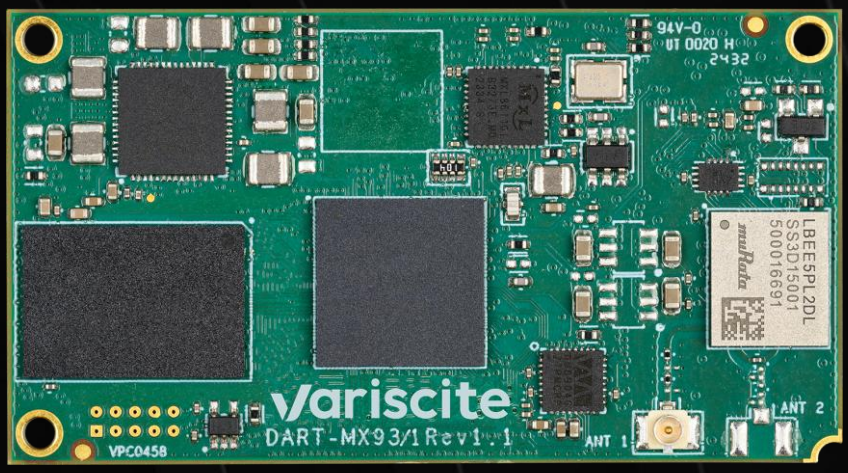
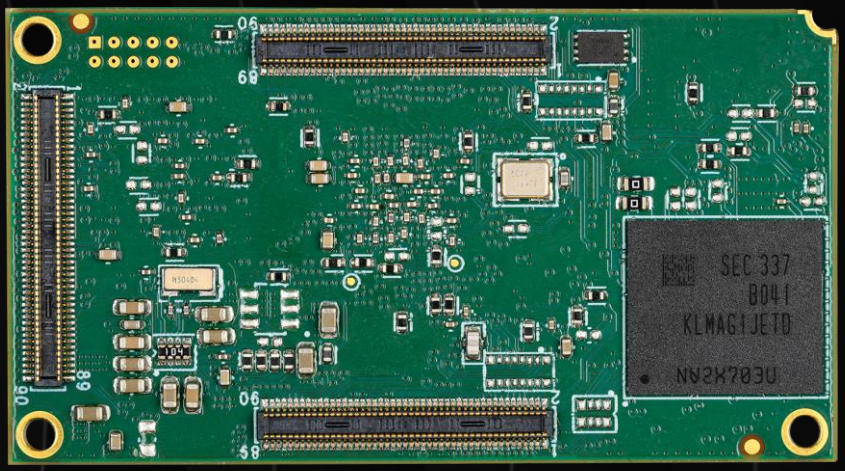
Rev. 1.4, 1/2026

VARISCITE LTD.

DART-MX91 Datasheet

NXP i.MX 91™ - based System-on-Module





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DART-MX91 Datasheet

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1. Document Revision History

Revision	Date	Notes
1.0	Feb 2, 2025	Initial Release
1.1	Mar 15, 2025	Processor Features updated to single core
1.2	Mar 26, 2025	Fixed J1.9 connection in EC assembly
1.3	Jan 22, 2026	Updated section 10.4
1.4	Jan 27, 2026	Corrected pin names J1.52,55,58,61,70 in case of default assembly

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4. Overview

4.1 General Information

DART-MX91 offers high-performance processing for a low-power System-on-Module. The product is based on the i.MX 91 family, which represents NXP's latest power-optimized processors for smart home, building control, contactless HMI, IoT edge, and Industrial applications.

The i.MX 91 applications processor features an Arm® Cortex®-A55 running at up to 1.4 GHz and support for modern LPDDR4 memory to enable platform longevity and reliability; dual Gigabit Ethernet for gateway or multi-network segment support; dual USB ports; and the essential I/O for products in smart factory, smart home, smart office, medical device, metering, and cost-optimized system-on-module platforms.

The DART-MX91 provides an ideal building block for simple integration with a wide range of products in target markets requiring high-performance processing with low power consumption, compact size, and a cost-effective solution.

Supporting products:

- DT8M Custom Board – evaluation board
  - ✓ Carrier Board, compatible with DART-MX91
  - ✓ Schematics
- VAR-DVK-DT91 full development kit, including:
  - ✓ DT8M Custom Board
  - ✓ DART-MX91
  - ✓ Display and touch
  - ✓ Accessories and cables
- O.S support
  - ✓ Linux BSP

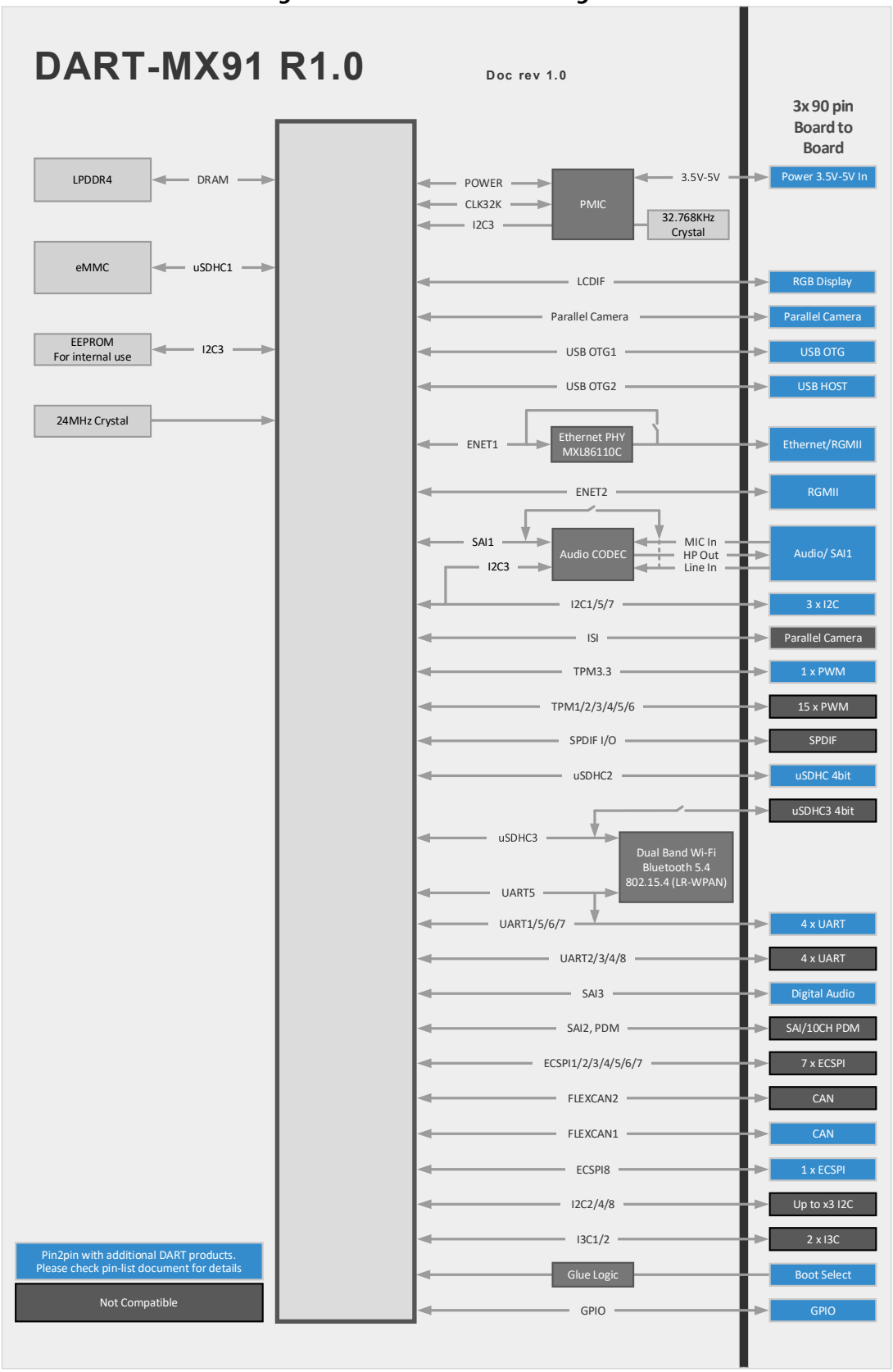
Contact Variscite support services for further information: support@variscite.com.

4.2 Feature Summary

- Cortex®-A55 MPCore platform
  - Two Cortex®-A55 processors operating up to 1.7 GHz
  - Media Processing Engine (MPE) with Arm® NEONTM technology supporting the Advanced Single Instruction Multiple Data architecture
  - Floating Point Unit (FPU) with support of the Arm® VFPv4-D16 architecture
  - Support of 64-bit Arm® v8.2-A architecture
  - 256 KB cluster L2 cache
  - Parity/ECC protection on L1 cache, L2 cache, and TLB RAMs
- Image Sensor Interface (ISI)
  - Standard pixel formats commonly used in many camera input protocols
  - Programmable resolutions up to 2K
  - Image processing for:
    - Supports one source of up to 2K horizontal resolution
    - Supports pixel rate up to 200 Mpixel/s
  - Image down scaling via decimation and bi-phase filtering
  - Color space conversion
  - Interlaced to progressive conversions
- On-chip memory
  - Boot ROM (256 KB) for Cortex®-A55
  - On-chip RAM (384 KB)
- RAM memory
  - Up to 2GBytes of LPDDR4 RAM
- Storage
  - Up to 128GBytes of eMMC5.1 (8bit) interface supporting up to 400MB/sec
- Pixel Pipeline (PXP)
  - Flexible image composition options—alpha, chroma key
  - Porter-Duff operation
  - Image rotation (90o, 180o, 270o)
  - Image resize
  - Color space conversion
  - Multiple pixel format support (RGB, YUV444, YUV422, YUV420, YUV400)
  - Standard 2D-DMA operation
- LCDIF Display Controller
  - The LCDIF can drive any parallel LCD up to 1366x768p60 or 1280x800p60 resolution
- Other Interfaces
  - SDIO/MMC
  - Resistive touch controller
  - Serial interfaces (ECSPI, FlexSPI, I2C, UART, CAN, JTAG, SAI)
  - GPIOs
- Single power supply: 3.5V - 5V
- Dimensions (W x L x H): 30 mm x 55 mm x 5.13 mm
- Industrial temperature range: -40ºC to 85ºC

4.3 Block Diagram

Figure 1 : DART-MX91 Block Diagram



5. Main Hardware Components

This section summarizes the main hardware building blocks of the DART-MX91.

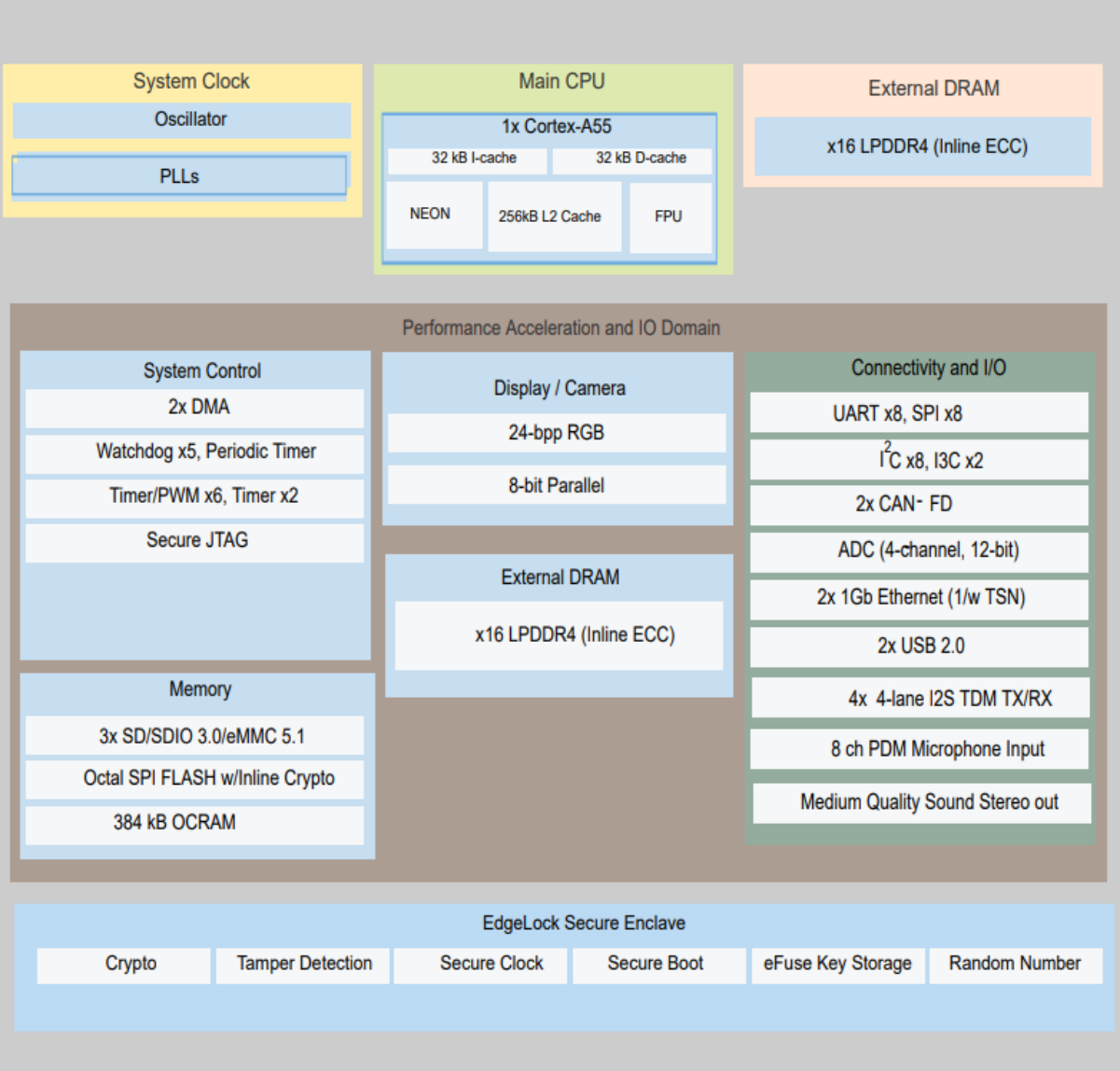
5.1 NXP i.MX 91

5.1.1 Overview

The i.MX 91 family of applications processors enables the rapid creation of new Linux®-based edge devices, such as smart home controllers, connected appliances, home entertainment, industrial, and medical platforms. Emerging protocols, such as Matter™ for the smart home or the ISO 15118-20 standard for electric vehicle (EV) chargers, create inflection points for new product categories across IoT and industrial markets. Next-generation Linux-based devices based on i.MX 91 SoC will be high-performance, affordable, and secure solutions, enabling adaption to updated protocols or new standards as they are introduced. The i.MX 91 SoC's integrated EdgeLock® Secure Enclave provides security features, including lifecycle management, tamper detection, secure boot, and a simplified path to certifications. The i.MX 91 family features an Arm® Cortex®-A55 running at up to 1.4GHz, support for modern LPDDR4 memory to enable platform longevity, dual Gigabit Ethernet, and dual USB ports, along with a rich set of peripherals targeting medical, industrial and consumer IoT market segments. Part of the EdgeVerse™ portfolio of intelligent edge solutions, the i.MX 91 family will be offered in consumer and industrial qualification and backed by NXP's product longevity program.

5.1.2i.MX91 Block Diagram

Figure 2 : i.MX91 Block Diagram



5.1.3 Arm Cortex®-A55 MPCore cluster

- One cluster of Cortex-A55 cores
- The core includes 32kB L1-I, 32kB L1-D and 256kB L2 cache
- Core cache protection (parity/ECC) supported

5.1.4 On Chip Memory

- Boot ROM (256KB)
- 384KB of SoC-specific OCRAM

5.1.5 External Memory

- One 16-bit DRAM controller:
  - Maximum supported capacity is 2GByte
  - LPDDR4 supported

5.1.6 Graphics

- LCDIF display
  - Parallel display (up to 1366x768 or 1280x800)
- ISI camera interface
  - Parallel camera

5.1.7 Audio

- SPDIF supports raw capture mode that can save all the incoming bits into audio buffer.
- Up to 3x Synchronous Audio Interface (SAI) modules supporting I2S, AC97, TDM, and Codec/DSP interfaces
- Digital microphone input, up to 8-channel PDM

Note: *The above list refers to the chip capabilities, part of the pins is used on the SOM therefore the exact number of interfaces can be lower.*

5.1.8Connectivity

- 2x USB 2.0 OTG controller with integrated PHY interfaces
- 3x Ultra Secure Digital Host Controller (uSDHC) interfaces
    - uSDHC1 with boot support for eMMC 5.1 compliance with HS400 DDR signaling to support up to 400 MB/sec
    - uSDHC2 with boot support for SD/SDIO 3.0 compliance with 200 MHz SDR signaling to support up to 100 MB/sec
    - Support for SDXC (extended capacity)
    - USDHC3 to support use cases that need simultaneous support for all three of 1x eMMC, 1x SD Card and 1x SDIO (for WIFI connectivity)
- Up to 8x Universal asynchronous receiver/transmitter (LPUARTs) modules
- Up to 8x LPSPI modules
- Up to 8x I2C modules
- Up to 2x I3C modules
- Up to 2x CAN-FD modules
- Up to 1x 1G-bit Ethernet with AVB support (ENET)
- 1x 1G-bit Ethernet with AVB, QoS Support (Ethernet QoS)

Note: *The above list refers to the chip capabilities, part of the pins is used on the SOM therefore the exact number of interfaces can be lower.*

5.1.9Timers and PWMs

- 2x Low Power Periodical Interrupt Timer (LPIT)
    - 4 channels
    - 4 external trigger sources
    - Generic 32-bit resolution timer
    - Periodical interrupt generation
- 6x Timer/PWM module (TPM)
    - Prescaler divide-by 1, 2, 4, 8, 16, 32, 64, or 128
    - 16-bit counter, support free-running counter or modulo counter mode, counting-up or down
    - Includes 6 channels that can be configured for input capture, output compare, edge-aligned PWM mode, or center aligned PWM mode
- 2x Low-Power Timer (LPTMR)
- 5x WatchDog modules (WDOG)

Note: *The above list refers to the chip capabilities, part of the pins is used on the SOM therefore the exact number of interfaces can be lower.*

5.1.10 GPIO and Pin Multiplexing:

- General-purpose input/output (GPIO) modules with interrupt capability
- Input/output multiplexing controller (IOMUXC) to provide centralized pad control

5.1.11 Analog:

- 1x 12-bit Analog Digital Converter (ADC)

5.1.12 Security:

- TRDC – Resource Domain Controller

    - Supports up to 16 resource domains
- Arm TrustZone® (TZ) architecture
- Secure and trusted access control
- Battery Backed Security Module (BBSM)
    - Monotonic counter - Secure real-time clock (RTC) - Zeroizable Master Key

5.1.13 System Debug

- Arm CoreSight® debug and trace architecture
- Trace Port Interface Unit (TPIU) to support off-chip real-time trace
- Support for 5-pin (JTAG) and SWD debug interfaces

5.1.14 Power Management

- One PMIC to supply all power rails.
- Temperature sensor with programmable trim points
- GPC hardware power management controller
    -

5.2 Memory

5.2.1RAM

The DART-MX91 is available with up to 2GB of LPDDR4 memory.

5.2.2Non-volatile Storage Memory

The DART-MX91 is available with a non-volatile MLC eMMC storage memory with optional densities of up to 128GB. It is used for Flash Disk purposes, O.S. run-time images, Bootloaders, and application/user data storage.

5.3 Audio (WM8904)

The WM8904 is a high performance ultra-low power stereo CODEC optimized for portable audio applications.
The device features stereo ground-referenced headphone amplifiers using the Wolfson 'Class-W' amplifier techniques. It incorporates an innovative dual-mode charge pump architecture - to optimize efficiency and power consumption during playback.
The ground-referenced headphone output eliminates AC coupling capacitors, and both outputs include common mode feedback paths to reject ground noise. Control sequences for audio path setup can be pre-loaded and executed by an integrated control write sequencer to reduce software driver development and minimize pops and clicks via SilentSwitch™ technology. The input impedance is constant with PGA gain setting. A stereo digital microphone interface is provided, with a choice of two inputs. A dynamic range controller provides compression and level control to support a wide range of portable recording applications. Anti-clip and quick release features offer good performance in the presence of loud impulsive noises. ReTuneTM Mobile 5-band parametric equalizer with fully programmable coefficients is integrated for optimization of speaker characteristics. Programmable dynamic range control is also available for maximizing loudness, protecting speakers from clipping, and preventing premature shutdown due to battery droop. Common audio sampling frequencies are supported from a wide range of external clocks, either directly or generated via the FLL.

Features:

- 3.0mW quiescent power consumption for DAC to headphone playback
- DAC SNR 96dB typical, THD -86dB typical
- ADC SNR 91dB typical, THD -80dB typical
- 2.4mW quiescent power consumption for analogue bypass playback
- Control write sequencer for pop minimized start-up and shutdown
- Single register writes for default start-up sequence
- Integrated FLL provides all necessary clocks - Self-clocking modes allow processor to sleep - All standard sample rates from 8kHz to 96kHz
- Stereo digital microphone input
- 2 single ended inputs per stereo channel
- Digital Dynamic Range Controller (compressor / limiter)
- Digital sidetone mixing
- Ground-referenced headphone driver

5.4 Wi-Fi + BT + LR-WPAN

DART-MX91 module can be configured either for using one of two Wi-Fi modules based on NXP chipset:

- 2.4GHz & 5GHz Wi-Fi® + Bluetooth® + 802.15.4 Module based on NXP IW612 chipset
- 2.4GHz & 5GHz Wi-Fi® + Bluetooth® Module based on NXP IW611 chipset

Both realize the necessary PHY/MAC layers to support WLAN applications in conjunction with a host processor over a SDIO interface.
The modules also provide a Bluetooth/BLE platform through the HCI transport layer. Both WLAN and Bluetooth share the same antenna port or may be ordered with dual antenna ports.
The SOM can be ordered with 802.15.4 low-rate wireless personal area network (LR-WPAN)

DART-MX91 Wi-Fi Key Features:

- 1x1 2.4/5 GHz, up to 80 MHz channel
- UL/DL MU-MIMO and OFDMA
- Target Wake Time, Dual Carrier Modulation, Extended Range
- 802.11az accurate ranging
- WPA3 security

DART-MX91 Bluetooth Key Features:

- Supports Bluetooth 5.4
- Integrated high power PA up to +20dBm transmit power
- Full featured Bluetooth baseband
- SCO/eSCO links with hardware accelerated audio signal processing
- Bluetooth LE 2 Mbit/s, Long Range, Advertising Extensions
- LE Audio with Isochronous channels (I2S/PCM)

DART-MX91 802.15.4 Key Features:

- IEEE 802.15.4-2015 compliant supporting Thread in 2.4 GHz band
- Integrated high power PA up to +20 dBm transmit power
- Shared transmitter and antenna pin with Bluetooth
- Simultaneous receive with Bluetooth

5.4.1DART-MX91 2.4GHz & 5GHz Wi-Fi® + Bluetooth® + 802.15.4 Option

The DART-MX91 contains Murata's certified high-performance Type 2EL Module based upon the NXP IW612 chipset supporting Wi-Fi® 11a/b/g/n/ac/ax + Bluetooth® 5.4 + 802.15.4 wireless connectivity.

5.4.2DART-MX91 2.4GHz & 5GHz Wi-Fi® + Bluetooth® Option

The DART-MX91 contains Murata's certified high-performance Type 2DL Module based upon the NXP IW611 chipset supporting Wi-Fi® 11a/b/g/n/ac/ax + Bluetooth® 5.4 wireless connectivity.

5.5 PMIC

The DART-MX91 features NXP's PCA9541 chip as a Power Management Integrated circuit (PMIC) designed specifically for use with NXP's i.MX 91 series of application processors. The PCA9541 regulates power rails required on SOM from a single 3.3V power supply.

The PMIC is fully programmable via the I2C interface and associated register map.
Additional communication is provided by direct logic interfacing including interrupt, watchdog and reset.

5.6 10/100/1000 Mbps Ethernet Transceiver

The DART-MX91 features on board an MXL86110C or MXL86110I Integrated Ethernet Transceiver.
Key features include:

- 1000BASE-T (IEEE 802.3), 100BASE-TX (IEEE 802.3) and 10BASE-Te (IEEE 802.3)
- Ethernet twisted pair copper cable of category CAT5 or higher
- Low EMI voltage mode line driver with integrated termination resistors
- Transformer less Ethernet for backplane applications
- Auto-Negotiation (ANEG) with extended next page support
- Auto-MDIX and polarity correction
- Auto-Down speed (ADS)
- Energy-Efficient Ethernet (EEE) and power down mode
- Wake-on-LAN (WoL)
- 10k byte jumbo frame support
- RGMII Interface
- An MDIO slave interface supports IEEE 802.3 Clause 22 and Clause 45
- An MDIO interface clock of up to 12.5 MHz
- Three MDIO message frame types: Clause 22, Clause 22 Extended, and Clause 45
- Two fully programmable LEDs

5.7 EEPROM

The DART-MX91 uses 4Kbit serial EEPROM to store memory calibration and manufacturing parameters.
This EEPROM is connected to I2C3 bus and intended only for holding the above information.
The SOM may not boot if the contents of EEPROM device are corrupted.

6. DART-MX91 Hardware Configuration

The table below lists the Hardware configurations options orderable for the DART-MX91.

Table 1: Hardware Configuration Options

Option	Description
EC	Ethernet PHY assembled on SOM
AC	Audio Codec assembled on SOM
WBE	2.4GHz & 5GHz Wi-Fi® + Bluetooth® + 802.15.4 Module assembled on SOM
WBD	2.4GHz & 5GHz Wi-Fi® + Bluetooth® Module assembled on SOM
COEX	Expose WCI-2 coexistence management lines needed only in case another RF part should be synchronised with the internal Wi-Fi module
BTRST	Expose Bluetooth® and 802.15.4 reset lines
ANT2	Dual antenna mode. ANT1 for Wi-Fi, ANT2 for BT and 802.15.4
WRST	Expose 2.4GHz & 5GHz Wi-Fi® reset line needed only for disabling the RF in HW
SDEX	Expose uSDHC3 interface, available only when no WBD/WBE is selected

Note 1: *Additional orderable options may be available that are not included in this datasheet. For a complete list of configuration options, please visit the Variscite official website or contact their sales personnel.*

7. External Connectors

7.1 Board to Board Connector

- The DART-MX91 exposes three 90-pin board-to-board connectors.
- The recommended mating connector is: **Hirose Electric Co Ltd PN: DF40C-90DS-0.4V(51)**

7.2 Wi-Fi & BT, 802.15.4 Connector

In Modules with Wi-Fi "WBE" or "WBD" Configuration - a combined Wi-Fi + BT antenna connector is assembled. In case of "ANT2" Configuration dual Antenna connectors are assembled.

- Connector type: U.FL JACK connector
- Cable and antenna shall have a 50 Ohm characteristic impedance

7.3 DART-MX91 Connector Pin-out

Table 2: DART-MX91 Pinout

Pin	Assembly Option	Pad Name	Notes	GPIO	Ball
J1.1		PMIC_NINT	Runs @ 1.8V. Has an internal 100K pull up.		PCA9451.13
J1.2	EC	ETH0_MDI_B_P			MxL86110x.4
J1.2	Non-EC	ENET1_TD1	Runs @ 1.8V.	GPIO4_IO4	SOC.T12
J1.3	EC	NC			
J1.3	Non-EC	ENET1_TX_CTL	Runs @ 1.8V.	GPIO4_IO6	SOC.V10
J1.4	EC	ETH0_MDI_B_M			MxL86110x.5
J1.4	Non-EC	ENET1_TD0	Runs @ 1.8V.	GPIO4_IO5	SOC.W11
J1.5	EC	LED_LINK10_100	Connected to GND		
J1.5	Non-EC	ENET1_TXC	Runs @ 1.8V.	GPIO4_IO7	SOC.U10
J1.6	EC	ETH0_MDI_A_M			MxL86110x.2
J1.6	Non-EC	ENET1_TD2	Runs @ 1.8V.	GPIO4_IO3	SOC.U12
J1.7	EC	ETH0_LED_LINK			MxL86110x.33
J1.7	Non-EC	ENET1_RXC	Runs @ 1.8V. Has EMI filter.	GPIO4_IO9	SOC.AA7
J1.8	EC	ETH0_MDI_A_P			MxL86110x.1
J1.8	Non-EC	ENET1_TD3	Runs @ 1.8V.	GPIO4_IO2	SOC.V12
J1.9	EC	ETH0_LED_ACT			MxL86110x.34
J1.9	Non-EC	ENET1_RX_CTL	Runs @ 1.8V.	GPIO4_IO8	SOC.Y8
J1.10	EC	ETH0_MDI_C_P			MxL86110x.6
J1.10	Non-EC	ENET1_RD0	Runs @ 1.8V.	GPIO4_IO10	SOC.AA8
J1.11		ENET1_MDIO	Runs @ 3.3V. Routed through PMIC internal voltage translator. Has an internal 1.47K pull up.	GPIO4_IO1	SOC.AA10
J1.12	EC	ETH0_MDI_C_M			MxL86110x.7
J1.12	Non-EC	ENET1_RD1	Runs @ 1.8V.	GPIO4_IO11	SOC.Y9
J1.13		ENET1_MDC	Runs @ 3.3V. Routed through PMIC internal voltage translator. Has an internal 1.47K pull up.	GPIO4_IO0	SOC.AA11
J1.14	EC	ETH0_MDI_D_P			MxL86110x.9
J1.14	Non-EC	ENET1_RD2	Runs @ 1.8V.	GPIO4_IO12	SOC.AA9
J1.15		NVCC_BBSM			PCA9451.3
J1.16	EC	ETH0_MDI_D_M			MxL86110x.10
J1.16	Non-EC	ENET1_RD3	Runs @ 1.8V.	GPIO4_IO13	SOC.Y10
J1.17		GPIO_IO07		GPIO2_IO7	SOC.L21
J1.18		GND			
J1.19		GPIO_IO06		GPIO2_IO6	SOC.L20
J1.20		ONOFF	Runs @ 1.8V.		SOC.A19
J1.21		GND			

Pin	Assembly Option	Pad Name	Notes	GPIO	Ball
J1.22		PMIC_RST_B	Runs @ 1.8V. Pull low to hold DART internal regulators OFF. Pulse low for cold reboot. Has an internal 100K pull up.		PCA9451.8
J1.23	WBD/WBE	BT_HOST_WAKE	Runs @ 1.8V.		LBES5PL2xL.76
J1.23	Non-WBD/WBE	NC			
J1.24		POR_B	Runs @ 1.8V. Pull low to hold SOC in reset state. Pulse low for Warm reboot. Has an internal 100K pull up.		PCA9451.9
J1.25	WBD/WBE	WIFI_HOST_WAKE	Runs @ 1.8V.		LBES5PL2xL.73
J1.25	Non-WBD/WBE	NC			
J1.26		PMIC_STBY_REQ	Runs @ 1.8V.		SOC.B18
J1.27		VDD_3V3	Power output from PMIC. Recommend to use as base board 3.3V regulator enable.		PCA9451.19
J1.28		CCM_CLKO3	Runs @ 1.8V.	GPIO4_IO28	SOC.U4
J1.29		NC			
J1.30		GND			
J1.31		NC			
J1.32	WBD/WBE	BT_DEV_WAKE	Runs @ 1.8V.		LBES5PL2xL.75
J1.32	Non-WBD/WBE	NC			
J1.33		GND			
J1.34		NC			
J1.35		NC			
J1.36	WBD/WBE	BT_PCM_IN	Runs @ 1.8V.		LBES5PL2xL.91
J1.36	Non-WBD/WBE	NC			
J1.37		NC			
J1.38		NC			
J1.39	WBD/WBE	RF_CNTL1	Runs @ 1.8V.		LBES5PL2xL.26
J1.39	Non-WBD/WBE	NC			
J1.40		NC			
J1.41		NC			
J1.42		NC			
J1.43		NC			
J1.44		NC			
J1.45		NC			
J1.46		NC			
J1.47		NC			
J1.48		NC			
J1.49		GND			
J1.50		NC			
J1.51		NC			

Pin	Assembly Option	Pad Name	Notes	GPIO	Ball
J1.52	BTRST	BT_KILL	Runs @ 1.8V.		LBES5PL2xL.64
J1.52	Non-BTRST	GND			
J1.53		NC			
J1.54	WBD/WBE	BT_PCM_CLK	Runs @ 1.8V.		LBES5PL2xL.57
J1.54	Non-WBD/WBE	NC			
J1.55	WBD/WBE	WLAN_SPI_CS0	Runs @ 1.8V.		LBES5PL2xL.4
J1.55	Non-WBE	GND			
J1.56	WBD/WBE	BT_PCM_OUT	Runs @ 1.8V.		LBES5PL2xL.59
J1.56	Non-WBD/WBE	NC			
J1.57		NC			
J1.58	WRST	WB_KILL	Runs @ 1.8V.		LBES5PL2xL.63
J1.58	Non-WRST	GND			
J1.59		NC			
J1.60		NC			
J1.61	WBE	WLAN_SPI_RXD	Runs @ 1.8V.		LBES5PL2xL.6
J1.61	Non-WBE	GND			
J1.62		NC			
J1.63	WBE	WLAN_SPI_TXD	Runs @ 1.8V.		LBES5PL2xL.7
J1.63	Non-WBE	NC			
J1.64	WBD/WBE	RF_CNTL0	Runs @ 1.8V.		LBES5PL2xL.27
J1.64	Non-WBD/WBE	GND			
J1.65	WBD/WBE	BT_PCM_SYNC	Runs @ 1.8V.		LBES5PL2xL.61
J1.65	Non-WBD/WBE	NC			
J1.66	WBD/WBE	RF_CNTL3	Runs @ 1.8V.		LBES5PL2xL.25
J1.66	Non-WBD/WBE	NC			
J1.67	WBE	WLAN_SPI_CLK	Runs @ 1.8V.		LBES5PL2xL.8
J1.67	Non-WBE	GND			
J1.68	WBD/WBE	RF_CNTL4	Runs @ 1.8V.		LBES5PL2xL.24
J1.68	Non-WBD/WBE	NC			
J1.69		NC			
J1.70	BTRST	LR_KILL	Runs @ 1.8V.		LBES5PL2xL.38
J1.70	Non-BTRST	GND			
J1.71		NC			
J1.72		NC			
J1.73		NC			
J1.74		SD2_CD_B	External SD card detect input. Will change level according to J1.90 NVCC_SD.	GPIO3_IO0	SOC.Y17
J1.75		NC			
J1.76		GND			
J1.77		NC			

Pin	Assembly Option	Pad Name	Notes	GPIO	Ball
J1.78		SD2_DATA2	Will change level according to J1.90 NVCC_SD.	GPIO3_IO5	SOC.Y20
J1.79		NC			
J1.80		SD2_DATA1	Will change level according to J1.90 NVCC_SD.	GPIO3_IO4	SOC.AA18
J1.81		NC			
J1.82		SD2_CLK	Will change level according to J1.90 NVCC_SD.	GPIO3_IO1	SOC.AA19
J1.83		NC			
J1.84		SD2_DATA3	Will change level according to J1.90 NVCC_SD.	GPIO3_IO6	SOC.AA20
J1.85		GND			
J1.86		SD2_DATA0	Will change level according to J1.90 NVCC_SD.	GPIO3_IO3	SOC.Y18
J1.87		NC			
J1.88		SD2_CMD	Will change level according to J1.90 NVCC_SD.	GPIO3_IO2	SOC.Y19
J1.89		NC			
J1.90		NVCC_SD	Power output for SD2 pins reference 1.8V/3.3V.		PCA9451.55
J2.1		NC			
J2.2	AC	HPLOUT	100nF and 20Ω Zobel network required		WM8904.13
J2.2	Non-AC	SAI1_RXD0		GPIO1_IO14	SOC.H20
J2.3		NC			
J2.4	AC	HPROUT	100nF and 20Ω Zobel network required		WM8904.15
J2.4	Non-AC	SAI1_TXC		GPIO1_IO12	SOC.G20
J2.5		NC			
J2.6	AC	HPOUTFB			WM8904.14
J2.6	Non-AC	I2C2_SCL		GPIO1_IO2	SOC.D20
J2.7		NC			
J2.8	AC	LINEIN1_LP			WM8904.26
J2.8	Non-AC	I2C2_SDA		GPIO1_IO3	SOC.D21
J2.9		NC			
J2.10	AC	LINEIN1_RP			WM8904.24
J2.10	Non-AC	SAI1_TXFS	BOOT_MODE2 pin. Has an internal SOC PD. Do not drive until after POR_B rise + 30ms	GPIO1_IO11	SOC.G21
J2.11		NC			
J2.12		AGND			
J2.13		NC			
J2.14	AC	DMIC_CLK	DMIC output.		WM8904.1
J2.14	Non-AC	SAI1_TXD0	BOOT_MODE3 pin. Has an internal SOC PD. Do not drive until after POR_B rise + 30ms.	GPIO1_IO13	SOC.H21
J2.15		NC			
J2.16	AC	DMIC_DATA	Runs @ 1.8V. DMIC input.		WM8904.27
J2.16	Non-AC	UART2_RXD		GPIO1_IO6	SOC.F20
J2.17		NC			

Pin	Assembly Option	Pad Name	Notes	GPIO	Ball
J2.18		GND			
J2.19		NC			
J2.20		DAP_TDO_TRACESWO	Runs @ 1.8V. Used on DART for BT communication. Pin can be used when BT disabled.	GPIO3_IO31	SOC.Y2
J2.21		NC			
J2.22		DAP_TMS_SWDIO	Runs @ 1.8V. Used on DART for BT communication. Pin can be used when BT disabled.	GPIO3_IO29	SOC.W2
J2.23		GND			
J2.24		DAP_TDI	Runs @ 1.8V. Used on DART for BT communication. Pin can be used when BT disabled.	GPIO3_IO28	SOC.W1
J2.25	SDEX	SD2_RESET_B	Runs @ J1.90 VDD_SDIO2 level.	GPIO3_IO7	SOC.AA17
J2.25	Non-SDEX	NC			
J2.26		DAP_TCLK_SWCLK	Runs @ 1.8V. Used on DART for BT communication. Pin can be used when BT disabled.	GPIO3_IO30	SOC.Y1
J2.27	SDEX	ENET2_MDIO	Runs @ 1.8V.	GPIO4_IO15	SOC.AA6
J2.27	Non-SDEX	NC			
J2.28		WDOG_ANY		GPIO1_IO15	SOC.J18
J2.29	SDEX	SD3_DATA3	Runs @ 1.8V.	GPIO3_IO25	SOC.T14
J2.29	Non-SDEX	NC			
J2.30		I2C1_SDA		GPIO1_IO1	SOC.C21
J2.31	SDEX	SD3_DATA2	Runs @ 1.8V.	GPIO3_IO24	SOC.U14
J2.31	Non-SDEX	NC			
J2.32		I2C1_SCL		GPIO1_IO0	SOC.C20
J2.33	SDEX	SD3_DATA1	Runs @ 1.8V.	GPIO3_IO23	SOC.V14
J2.33	Non-SDEX	NC			
J2.34		GPIO_IO19		GPIO2_IO19	SOC.R17
J2.35	SDEX	SD3_DATA0	Runs @ 1.8V.	GPIO3_IO22	SOC.T16
J2.35	Non-SDEX	NC			
J2.36		GPIO_IO20		GPIO2_IO20	SOC.T20
J2.37	COEX	COEX_SIN	Runs @ 1.8V.		LBES5PL2xL.69
J2.37	Non-COEX	NC			
J2.38		GPIO_IO16		GPIO2_IO16	SOC.R21
J2.39	COEX	COEX_SOUT	Runs @ 1.8V.		LBES5PL2xL.70
J2.39	Non-COEX	NC			
J2.40		GPIO_IO18		GPIO2_IO18	SOC.R18
J2.41		VDD			PCA9451.15
J2.42		GPIO_IO26		GPIO2_IO26	SOC.V20
J2.43	SDEX	SD3_CMD	Runs @ 1.8V.	GPIO3_IO21	SOC.U16
J2.43	Non-SDEX	NC			

Pin	Assembly Option	Pad Name	Notes	GPIO	Ball
J2.44		GPIO_IO21		GPIO2_IO21	SOC.T21
J2.45	SDEX	SD3_CLK	Runs @ 1.8V.	GPIO3_IO20	SOC.V16
J2.45	Non-SDEX	NC			
J2.46		GPIO_IO17		GPIO2_IO17	SOC.R20
J2.47		GND			
J2.48		GPIO_IO10		GPIO2_IO10	SOC.N17
J2.49		NC			
J2.50		PDM_CLK		GPIO1_IO8	SOC.G17
J2.51		NC			
J2.52		NC			
J2.53		GND			
J2.54		GPIO_IO27		GPIO2_IO27	SOC.W21
J2.55		NC			
J2.56		PDM_BIT_STREAM0		GPIO1_IO9	SOC.J17
J2.57		NC			
J2.58		NC			
J2.59		NC			
J2.60		GPIO_IO25		GPIO2_IO25	SOC.V21
J2.61		NC			
J2.62		NC			
J2.63		NC			
J2.64		ENET2_RX_CTL	Runs @ 1.8V.	GPIO4_IO22	SOC.Y4
J2.65		ENET2_RD0	Runs @ 1.8V.	GPIO4_IO24	SOC.AA4
J2.66		ENET2_RD2	Runs @ 1.8V.	GPIO4_IO26	SOC.AA5
J2.67		ENET2_TD1	Runs @ 1.8V.	GPIO4_IO18	SOC.U8
J2.68		ENET2_RD3	Runs @ 1.8V.	GPIO4_IO27	SOC.Y6
J2.69		ENET2_RD1	Runs @ 1.8V.	GPIO4_IO25	SOC.Y5
J2.70		ENET2_TD0	Runs @ 1.8V.	GPIO4_IO19	SOC.T8
J2.71		ENET2_TXC	Runs @ 1.8V.	GPIO4_IO21	SOC.U6
J2.72		ENET2_RXC	Runs @ 1.8V.	GPIO4_IO23	SOC.AA3
J2.73		ENET2_TD3	Runs @ 1.8V.	GPIO4_IO16	SOC.T10
J2.74		ENET2_TX_CTL	Runs @ 1.8V.	GPIO4_IO20	SOC.V6
J2.75		GND			
J2.76		CCM_CLKO1	Runs @ 1.8V. Has an internal 12K pull down.	GPIO3_IO26	SOC.AA2
J2.77		GPIO_IO15		GPIO2_IO15	SOC.P21
J2.78		ENET2_TD2	Runs @ 1.8V. Internal buffer connected to this pin. It drives BOOT_MODE0, latched with POR_B rise.	GPIO4_IO17	SOC.V8
J2.79		GPIO_IO12		GPIO2_IO12	SOC.N20
J2.80		GPIO_IO11		GPIO2_IO11	SOC.N18

Pin	Assembly Option	Pad Name	Notes	GPIO	Ball
J2.81		GPIO_IO13		GPIO2_IO13	SOC.N21
J2.82	EC	ETH_INT	Runs @ 1.8V. Has an internal 1.47K pull up.		MxL86110x.31
J2.82	Non-EC	NC			
J2.83		GPIO_IO14		GPIO2_IO14	SOC.P20
J2.84		GND			
J2.85		GPIO_IO05		GPIO2_IO5	SOC.L18
J2.86		GPIO_IO04		GPIO2_IO4	SOC.L17
J2.87		GPIO_IO09		GPIO2_IO9	SOC.M21
J2.88		UART1_RXD	Used as console debug on Variscite release.	GPIO1_IO4	SOC.E20
J2.89		GPIO_IO8		GPIO2_IO8	SOC.M20
J2.90		UART1_TXD	Used as console debug on Variscite release. BOOT_MODE0 pin. Do not drive until after POR_B rise + 30ms. Internal buffer connected to J2.78 drives this pin. The sate latched with POR_B rise.	GPIO1_IO5	SOC.E21
J3.1		NC			
J3.2		NC			
J3.3		NC			
J3.4		NC			
J3.5		NC			
J3.6		NC			
J3.7		NC			
J3.8		NC			SOC.A4
J3.9		GND			
J3.10		GND			
J3.11		NC			
J3.12		NC			
J3.13		NC			
J3.14		NC			
J3.15		GND			
J3.16		NC			
J3.17		NC			
J3.18		NC			
J3.19		NC			
J3.20		NC			
J3.21		GND			
J3.22		NC			
J3.23		NC			
J3.24		GND			
J3.25		NC			
J3.26		USB2_VBUS	Runs @ 5.0V.		SOC.E14

Pin	Assembly Option	Pad Name	Notes	GPIO	Ball
			VBUS detect input		
J3.27		GND			
J3.28		NC			
J3.29		NC			
J3.30		GPIO_IO00		GPIO2_IO0	SOC.J21
J3.31		NC			SOC.E6
J3.32	WBE	WLAN_SPI_IRQ	Runs @ 1.8V. Has an internal 10K pullup.		LBES5PL2xL.5
J3.32	Non-WBE	NC			
J3.33		GND			
J3.34		GND			
J3.35		NC			
J3.36		NC			
J3.37		NC			
J3.38		GPIO_IO02		GPIO2_IO2	SOC.K20
J3.39		GND			
J3.40		NC			
J3.41		NC			
J3.42		GPIO_IO22		GPIO2_IO22	SOC.U18
J3.43		NC			
J3.44		USB2_ID	USB2 PHY native ID analogue input. Not recommended to use.		SOC.E12
J3.45		GND			
J3.46		GPIO_IO23		GPIO2_IO23	SOC.U20
J3.47		USB2_D_P			SOC.B15
J3.48		CCM_CLKO2	Runs @ 1.8V.	GPIO3_IO27	SOC.Y3
J3.49		USB2_D_N			SOC.A15
J3.50		GPIO_IO01		GPIO2_IO1	SOC.J20
J3.51		GND			
J3.52		CCM_CLKO4	Runs @ 1.8V.	GPIO4_IO29	SOC.V4
J3.53		NC			
J3.54		NC			
J3.55		NC			
J3.56		USB1_ID	USB2 PHY native ID analogue input. Not recommended to use.		SOC.C11
J3.57		GND			
J3.58		GPIO_IO03		GPIO2_IO3	SOC.K21
J3.59		NC			
J3.60		NC			
J3.61		NC			
J3.62		PDM_BIT_STREAM1		GPIO1_IO10	SOC.G18

Pin	Assembly Option	Pad Name	Notes	GPIO	Ball
J3.63		GND			
J3.64		GPIO_IO24		GPIO2_IO24	SOC.U21
J3.65		USB1_D_P			SOC.B14
J3.66		USB1_VBUS	Runs @ 5.0V. VBUS detect input.		SOC.F12
J3.67		USB1_D_N			SOC.A14
J3.68		GND			
J3.69		NC			
J3.70		TAMPER0	Runs @ 1.8V.		SOC.B16
J3.71		VBAT			
J3.72		TAMPER1	Runs @ 1.8V.		SOC.F14
J3.73		VBAT			
J3.74		GND			
J3.75		VBAT			
J3.76		ADC_IN0	Runs @ 1.8V.		SOC.B19
J3.77		VBAT			
J3.78		ADC_IN1	Runs @ 1.8V.		SOC.A20
J3.79		VBAT			
J3.80		ADC_IN2	Runs @ 1.8V.		SOC.B20
J3.81		VBAT			
J3.82		ADC_IN3	Runs @ 1.8V.		SOC.B21
J3.83		VBAT			
J3.84		CLKIN1	Runs @ 1.8V. Has an internal 100K pull down.		SOC.B17
J3.85		VBAT			
J3.86		CLKIN2	Runs @ 1.8V. Has an internal 100K pull down.		SOC.A18
J3.87		VBAT			
J3.88		PMIC_ON_REQ	Runs @ 1.8V.		SOC.A17
J3.89		VBAT			
J3.90		NC			

7.4 DART-MX91 Connector Pin Mux

Table 3: DART-MX91 PINMUX

Pin	Assy	Alt0	Alt1	Alt2	Alt3	Alt4	Alt5	Alt6	Alt7
J1.02	Non-EC	enet_qos.RGMII_TD1	uart3.RTS_B	i3c2.PUR	usb1.OTG_OC		gpio4.IO[4]	i3c2.PUR_B	
J1.03	Non-EC	enet_qos.RGMII_TX_CTL	uart3.DTR_B	spi2.SCK			gpio4.IO[6]		
J1.04	Non-EC	enet_qos.RGMII_TD0	uart3.TX				gpio4.IO[5]		
J1.05	Non-EC	enet_qos.RGMII_TXC	enet_qos.TX_ER	spi2.SIN			gpio4.IO[7]		
J1.06	Non-EC	enet_qos.RGMII_TD2	enet_qos.TX_CLK	can2.RX	usb2.OTG_OC		gpio4.IO[3]	i2c2.SDA	
J1.07	Non-EC	enet_qos.RGMII_RXC	enet_qos.RX_ER	spi2.SOUT			gpio4.IO[9]		
J1.08	Non-EC	enet_qos.RGMII_TD3		can2.TX	usb2.OTG_ID		gpio4.IO[2]	i2c2.SCL	
J1.09	Non-EC	enet_qos.RGMII_RX_CTL	uart3.DSR_B	spi2.PCS0	usb2.OTG_PWR		gpio4.IO[8]		
J1.10	Non-EC	enet_qos.RGMII_RD0	uart3.RX				gpio4.IO[10]		
J1.11		enet_qos.MDIO	uart3.RIN_B	i3c2.SDA	usb1.OTG_PWR		gpio4.IO[1]	i2c1.SDA	
J1.12	Non-EC	enet_qos.RGMII_RD1	uart3.CTS_B		lptmr2.ALT1		gpio4.IO[11]		
J1.13		enet_qos.MDC	uart3.DCD_B	i3c2.SCL	usb1.OTG_ID		gpio4.IO[0]	i2c1.SCL	
J1.14	Non-EC	enet_qos.RGMII_RD2			lptmr2.ALT2		gpio4.IO[12]		
J1.16	Non-EC	enet_qos.RGMII_RD3			lptmr2.ALT3		gpio4.IO[13]		
J1.17		gpio2.IO[7]	spi3.PCS1	isi.D[1]	lcdif.D[3]	spi7.SCK	uart6.RTS_B	i2c7.SCL	
J1.19		gpio2.IO[6]	tpm5.CH0	pdm.BIT_STREAM[1]	lcdif.D[2]	spi7.SOUT	uart6.CTS_B	i2c7.SDA	
J1.28		ccmsrcgpcmix.CLKO3					gpio4.IO[28]		
J1.74		usdhc2.CD_B	enet_qos.1588_EVENT0_IN	i3c2.SCL	i2c1.SCL		gpio3.IO[0]		sai3.TX_SYNC
J1.78		usdhc2.DATA2	enet2.1588_EVENT1_OUT	mqs2.RIGHT	uart2.TX		gpio3.IO[5]		
J1.80		usdhc2.DATA1	enet2.1588_EVENT1_IN	can2.RX	uart1.RX		gpio3.IO[4]		
J1.82		usdhc2.CLK	enet_qos.1588_EVENT0_OUT	i3c2.SDA	i2c1.SDA		gpio3.IO[1]		

Pin	Assy	Alt0	Alt1	Alt2	Alt3	Alt4	Alt5	Alt6	Alt7
J1.84		usdhc2.DATA3	lptmr2.ALT1	mqs2.LEFT	uart2.RX		gpio3.IO[6]		
J1.86		usdhc2.DATA0	enet2.1588_EVENT0_OUT	can2.TX	uart1.TX		gpio3.IO[3]		
J1.88		usdhc2.CMD	enet2.1588_EVENT0_IN	i3c2.PUR	i3c2.PUR_B		gpio3.IO[2]		
J2.02	Non-AC	sai1.RX_DATA[0]	sai1.MCLK	spi1.SOUT	uart2.DSR_B	mqs1.RIGHT	gpio1.IO[14]		
J2.04	Non-AC	sai1.TX_BCLK	uart2.CTS_B	spi1.SIN	uart1.DSR_B	can1.RX	gpio1.IO[12]		
J2.06	Non-AC	i2c2.SCL	i3c1.PUR	uart2.DCD_B	tpm2.CH2	sai1.RX_SYNC	gpio1.IO[2]	i3c1.PUR_B	
J2.08	Non-AC	i2c2.SDA		uart2.RIN_B	tpm2.CH3	sai1.RX_BCLK	gpio1.IO[3]		
J2.10	Non-AC	sai1.TX_SYNC	sai1.TX_DATA[1]	spi1.PCS0	uart2.DTR_B	mqs1.LEFT	gpio1.IO[11]		
J2.14	Non-AC	sai1.TX_DATA[0]	uart2.RTS_B	spi1.SCK	uart1.DTR_B	can1.TX	gpio1.IO[13]	sai1.MCLK	
J2.16	Non-AC	uart2.RX	uart1.CTS_B	spi2.SOUT	tpm1.CH2	sai1.MCLK	gpio1.IO[6]		
J2.20		dap.TDO_TRACESWO	mqs2.RIGHT		can2.RX		gpio3.IO[31]	uart5.TX	
J2.22		dap.TMS_SWDIO					gpio3.IO[29]	uart5.RTS_B	
J2.24		dap.TDI	mqs2.LEFT		can2.TX		gpio3.IO[28]	uart5.RX	
J2.25	SDEX	usdhc2.RESET_B	lptmr2.ALT2				gpio3.IO[7]		
J2.26		dap.TCLK_SWCLK					gpio3.IO[30]	uart5.CTS_B	
J2.27	SDEX	enet2.MDIO	uart4.RIN_B	sai2.RX_BCLK			gpio4.IO[15]	gpio4.IO[15]	
J2.28		wdog1.WDOG_ANY					gpio1.IO[15]		
J2.29	SDEX	usdhc3.DATA3	flexspi.A_DATA[3]	i2c4.SCL			gpio3.IO[25]		
J2.30		i2c1.SDA	i3c1.SDA	uart1.RIN_B	tpm2.CH1		gpio1.IO[1]		
J2.31	SDEX	usdhc3.DATA2	flexspi.A_DATA[2]	i2c4.SDA			gpio3.IO[24]		
J2.32		i2c1.SCL	i3c1.SCL	uart1.DCD_B	tpm2.CH0		gpio1.IO[0]		
J2.33	SDEX	usdhc3.DATA1	flexspi.A_DATA[1]	uart2.RTS_B			gpio3.IO[23]		
J2.34		gpio2.IO[19]	sai3.RX_SYNC	pdm.BIT_STREAM[3]	lcdif.D[15]	spi5.SIN	spi4.SIN	tpm6.CH2	sai3.TX_DATA[0]
J2.35	SDEX	usdhc3.DATA0	flexspi.A_DATA[0]	uart2.CTS_B			gpio3.IO[22]		
J2.36		gpio2.IO[20]	sai3.RX_DATA[0]	pdm.BIT_STREAM[0]	lcdif.D[16]	spi5.SOUT	spi4.SOUT	tpm3.CH1	

Pin	Assy	Alt0	Alt1	Alt2	Alt3	Alt4	Alt5	Alt6	Alt7
J2.38		gpio2.IO[16]	sai3.TX_BCLK	pdm.BIT_STREAM[2]	lcdif.D[12]	uart3.CTS_B	spi4.PCS2	uart4.CTS_B	
J2.40		gpio2.IO[18]	sai3.RX_BCLK	isi.D[9]	lcdif.D[14]	spi5.PCS0	spi4.PCS0	tpm5.CH2	
J2.42		gpio2.IO[26]	usdhc3.DATA2	pdm.BIT_STREAM[1]	lcdif.D[22]	tpm5.CH3	dap.TDI	spi8.PCS1	sai3.TX_SYNC
J2.43	SDEX	usdhc3.CMD	flexspi.A_SS0_B	uart1.RTS_B			gpio3.IO[21]		
J2.44		gpio2.IO[21]	sai3.TX_DATA[0]	pdm.CLK	lcdif.D[17]	spi5.SCK	spi4.SCK	tpm4.CH1	sai3.RX_BCLK
J2.45	SDEX	usdhc3.CLK	flexspi.A_SCLK	uart1.CTS_B			gpio3.IO[20]		
J2.46		gpio2.IO[17]	sai3.MCLK	isi.D[8]	lcdif.D[13]	uart3.RTS_B	spi4.PCS1	uart4.RTS_B	
J2.48		gpio2.IO[10]	spi3.SOUT	isi.D[4]	lcdif.D[6]	tpm4.EXTCLK	uart7.CTS_B	i2c8.SDA	
J2.50		pdm.CLK	mqs1.LEFT			lptmr1.ALT1	gpio1.IO[8]	can1.TX	
J2.54		gpio2.IO[27]	usdhc3.DATA3	can2.RX	lcdif.D[23]	tpm6.CH3	dap.TMS_SWDIO	spi5.PCS1	
J2.56		pdm.BIT_STREAM[0]	mqs1.RIGHT	spi1.PCS1	tpm1.EXTCLK	lptmr1.ALT2	gpio1.IO[9]	can1.RX	
J2.60		gpio2.IO[25]	usdhc3.DATA1	can2.TX	lcdif.D[21]	tpm4.CH3	dap.TCLK_SWCLK	spi7.PCS1	
J2.64		enet2.RGMII_RX_CTL	uart4.DSR_B	sai2.TX_DATA[0]			gpio4.IO[22]	isi.D[5]	
J2.65		enet2.RGMII_RD0	uart4.RX				gpio4.IO[24]	isi.D[7]	
J2.66		enet2.RGMII_RD2	uart4.CTS_B	sai2.MCLK	mqs2.RIGHT		gpio4.IO[26]	isi.D[9]	
J2.67		enet2.RGMII_TD1	uart4.RTS_B				gpio4.IO[18]	isi.D[1]	
J2.68		enet2.RGMII_RD3	spdif1.OUT	spdif1.IN	mqs2.LEFT		gpio4.IO[27]		
J2.69		enet2.RGMII_RD1	spdif1.IN				gpio4.IO[25]	isi.D[8]	
J2.70		enet2.RGMII_TD0	uart4.TX				gpio4.IO[19]	isi.D[2]	
J2.71		enet2.RGMII_TXC	enet2.TX_ER	sai2.TX_BCLK			gpio4.IO[21]	isi.D[4]	
J2.72		enet2.RGMII_RXC	enet2.RX_ER				gpio4.IO[23]	isi.D[6]	
J2.73		enet2.RGMII_TD3		sai2.RX_DATA[0]			gpio4.IO[16]	isi.FRAME_VALID	
J2.74		enet2.RGMII_TX_CTL	uart4.DTR_B	sai2.TX_SYNC			gpio4.IO[20]	isi.D[3]	
J2.76		ccmsrcgpcmix.CLKO1					gpio3.IO[26]		
J2.77		gpio2.IO[15]	uart3.RX	isi.D[7]	lcdif.D[11]	spi8.SCK	uart8.RTS_B	uart4.RX	

Pin	Assy	Alt0	Alt1	Alt2	Alt3	Alt4	Alt5	Alt6	Alt7
J2.78		enet2.RGMII_TD2	enet2.TX_CLK				gpio4.IO[17]	isi.LINE_VALID	
J2.79		gpio2.IO[12]	tpm3.CH2	pdm.BIT_STREAM[2]	lcdif.D[8]	spi8.PCS0	uart8.TX	i2c8.SDA	sai3.RX_SYNC
J2.80		gpio2.IO[11]	spi3.SCK	isi.D[5]	lcdif.D[7]	tpm5.EXTCLK	uart7.RTS_B	i2c8.SCL	
J2.81		gpio2.IO[13]	tpm4.CH2	pdm.BIT_STREAM[3]	lcdif.D[9]	spi8.SIN	uart8.RX	i2c8.SCL	
J2.83		gpio2.IO[14]	uart3.TX	isi.D[6]	lcdif.D[10]	spi8.SOUT	uart8.CTS_B	uart4.TX	
J2.85		gpio2.IO[5]	tpm4.CH0	pdm.BIT_STREAM[0]	lcdif.D[1]	spi7.SIN	uart6.RX	i2c6.SCL	
J2.86		gpio2.IO[4]	tpm3.CH0	pdm.CLK	lcdif.D[0]	spi7.PCS0	uart6.TX	i2c6.SDA	
J2.87		gpio2.IO[9]	spi3.SIN	isi.D[3]	lcdif.D[5]	tpm3.EXTCLK	uart7.RX	i2c7.SCL	
J2.88		uart1.RX	seco.RX	spi2.SIN	tpm1.CH0		gpio1.IO[4]		
J2.89		gpio2.IO[8]	spi3.PCS0	isi.D[2]	lcdif.D[4]	tpm6.CH0	uart7.TX	i2c7.SDA	
J2.90		uart1.TX	seco.TX	spi2.PCS0	tpm1.CH1		gpio1.IO[5]		
J3.30		gpio2.IO[0]		isi.PCLK	lcdif.PCLK	spi6.PCS0	uart5.TX	i2c5.SDA	
J3.38		gpio2.IO[2]	i2c4.SDA	isi.FRAME_VALID	lcdif.VSYNC	spi6.SOUT	uart5.CTS_B	i2c6.SDA	
J3.42		gpio2.IO[22]	usdhc3.CLK	spdif1.IN	lcdif.D[18]	tpm5.CH1	tpm6.EXTCLK	i2c5.SDA	
J3.46		gpio2.IO[23]	usdhc3.CMD	spdif1.OUT	lcdif.D[19]	tpm6.CH1		i2c5.SCL	
J3.48		ccmsrcgpcmix.CLKO2					gpio3.IO[27]		
J3.50		gpio2.IO[1]		isi.D[0]	lcdif.DE	spi6.SIN	uart5.RX	i2c5.SCL	
J3.52		ccmsrcgpcmix.CLKO4					gpio4.IO[29]		
J3.58		gpio2.IO[3]	i2c4.SCL	isi.LINE_VALID	lcdif.HSYNC	spi6.SCK	uart5.RTS_B	i2c6.SCL	
J3.62		pdm.BIT_STREAM[1]	m33.NMI	spi2.PCS1	tpm2.EXTCLK	lptmr1.ALT3	gpio1.IO[10]	ccmsrcgpcmix. EXT_CLK1	
J3.64		gpio2.IO[24]	usdhc3.DATA0		lcdif.D[20]	tpm3.CH3	dap.TDO_TRACESWO	spi6.PCS1	

Note [1]: *The UART5 interface is utilized internally for Bluetooth communication.*
To use UART5 externally, Bluetooth must be turned off, or a Non-WBD/WBE SOM should be employed.

Note [2]: *The USDHC3 interface is utilized internally for Wi-Fi communication.*

To use USDHC3 externally, Wi-Fi must be turned off, or a Non-WBD/WBE SOM should be employed.

Note [3]: *The SAI1 interface is utilized internally for Codec communication.*
To use SAI1 externally, Codec should be disabled in device tree, or a Non-AC SOM should be employed

Note [4]: *The ENET_QOS.MDIO bus is used internally for Ethernet PHY communication.*
When the EC SOM is employed, the functionality of these pins cannot be changed.
The signals are routed through a bidirectional voltage translator and have 1.47KΩ pull-ups, which may limit the bandwidth.

8. SOM's Interfaces

8.1 Trace Impedance

SOM traces are designed with the below table impedance list per signal group.
Table is a reference when you are updating or creating constraints in the PCB design tool to set up the impedances/trace widths.

Table 4: SOM Signal Group Traces Impedance

Signal Group	Impedance
All single ended signals	50 Ω Single ended
USB Differential signals	90 Ω Differential
Ethernet Differential signal	100 Ω Differential

8.2 Display Interfaces

The i.MX 91 SoC features an LCDIF for RGB Parallel Display up to 1366x768p60 or 1280x800p60.

8.2.1LCDIF

The LCD Interface (LCDIF) is a system master that fetches graphics stored in memory and displays them on a TFT LCD panel.

8.2.1.1 LCDIF Signals

Table 5: LCDIF Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
J3.50		lcdif.DE	3		SOC.L17
J2.86		lcdif.D[0]	3		SOC.P20
J2.83		lcdif.D[10]	3		SOC.L18
J2.77		lcdif.D[11]	3		SOC.P21
J2.38		lcdif.D[12]	3		SOC.R21
J2.46		lcdif.D[13]	3		SOC.R20
J2.40		lcdif.D[14]	3		SOC.R18
J2.34		lcdif.D[15]	3		SOC.R17
J2.36		lcdif.D[16]	3		SOC.T20
J2.44		lcdif.D[17]	3		SOC.T21
J3.42		lcdif.D[18]	3		SOC.U18
J3.46		lcdif.D[19]	3		SOC.U20
J2.85		lcdif.D[1]	3		SOC.L20
J3.64		lcdif.D[20]	3		SOC.U21
J2.60		lcdif.D[21]	3		SOC.V21
J2.42		lcdif.D[22]	3		SOC.V20
J2.54		lcdif.D[23]	3		SOC.W21
J1.19		lcdif.D[2]	3		SOC.L21
J1.17		lcdif.D[3]	3		SOC.M20
J2.89		lcdif.D[4]	3		SOC.M21
J2.87		lcdif.D[5]	3		SOC.N17
J2.48		lcdif.D[6]	3		SOC.N18
J2.80		lcdif.D[7]	3		SOC.N20
J2.79		lcdif.D[8]	3		SOC.N21
J2.81		lcdif.D[9]	3		SOC.J20
J3.58		lcdif.HSYNC	3		SOC.K21
J3.30		lcdif.PCLK	3		SOC.J21
J3.38		lcdif.VSYNC	3		SOC.K20

8.2.2ISI - Image Sensing Interface

The ISI module interfaces to a pixel link source to obtain the image data for processing in its pipeline channel. The pipeline processes the image line from a configured source and performs one or more functions that are configured by software, such as down scaling, color space conversion, de-interlacing, alpha insertion, and cropping and rotation (horizontal and vertical). The processed image is stored into programmable memory locations.
The ISI module implements limited flow control mechanism to control output from its internal buffer flushing or sourcing an image ROM memory. Depending on the format type, the ISI is capable of processing and storing one line of pixels from the incoming

The key features of the ISI include:

- Up to 2K resolution at 30 or 60 fps (24bpp) on each channel.
- Input sources:
    - 1 pixel link interface that can interface to 1 camera sensor.
    - System memory (AXI master, internally converted to pixel link interface).
- Each processing pipeline or channel can be assigned to the same or different pixel input source.
- Stream multiplexing
    - Simple de-interlacing methods supported for interlaced input sources:
        - Weaving
- Stream manipulation
    - Supported pixel formats of images to be stored into memory
        - RAW8, RAW10, RAW12, RAW14, RAW16, RAW32
        - RGB888, BGR888, RGB565, RGB 10-bit, BGR 10-bit
        - YUV444, YUV422, YUV420 (8-bit, 10-bit, 12-bit) in planar or semi-planar formats
        - More formats listed in the description of FORMAT field in the channel's IMG_CTRL register
    - Downscaling of input image via decimation and bilinear filtering
        - Decimation by 2, 4, or 8 supported
        - Bilinear filter further downscales by 1.0 to 2.0 (fractional downscaling)
    - Color Space Conversion (CSC)
        - RGB, YUV, YCbCr
        - User defined color space matrix-based conversion
    - Alpha channel insertion for RGB formats
        - Global alpha value
    - Separate rectangular region of interest (ROI) alpha value. ROI alpha value has higher priority than global alpha value.
        - Up to 4 ROI non-overlapping rectangles supported
    - Mirroring (Image fip): Horizontal and vertical flipping supported.
    - Frame awareness and frame skipping
        - Clean frame start and shutdown based on HSYNC and VSYNC
        - Buffer overrun protection
        - Buffer underrun deterministic behavior
- Stream output options
    - Output to memory
        - Input source is converted to and processed by the processing pipeline as YUV444 or RGB.
        - Processed images are outputted from pipeline and stored into memory location specified by software.

        - Full line storage is available at processing channel output before outputting data to AXI. This storage can automatically split or combine depending on the output format being used.
        - Dual buffered addresses are used in ping pong fashion with active buffer status indication.
        - Line and frame stored interrupt status are used for software to track progress of frame.
- Flow control
    - Panic indication is used for software and device to increase priority of its write transactions to avoid potential overflow in output buffers. Software can configure thresholds for panic indication.
    - When pixels are sourced from memory or input line buffers are flushed, software can select to program the rate at which pixels are sent out. By default, one pixel is sent out per clock.
    - Back pressure mechanism is used to stall the channel pipeline during line buffer flushing and sourcing image from memory when AXI bus is unable accept data and the output buffers are low on storage.
- Metadata processing
    - The embedded data from the sensor can be processed and written out.

8.2.2.1 ISI Signals

Table 6: ISI Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
J3.50		isi.D[0]	2		SOC.J20
J2.67		isi.D[1]	6	Runs @ 1.8V.	SOC.U8
J1.17		isi.D[1]	2		SOC.L21
J2.70		isi.D[2]	6	Runs @ 1.8V.	SOC.T8
J2.89		isi.D[2]	2		SOC.M20
J2.74		isi.D[3]	6	Runs @ 1.8V.	SOC.V6
J2.87		isi.D[3]	2		SOC.M21
J2.48		isi.D[4]	2		SOC.N17
J2.71		isi.D[4]	6	Runs @ 1.8V.	SOC.U6
J2.64		isi.D[5]	6	Runs @ 1.8V.	SOC.Y4
J2.80		isi.D[5]	2		SOC.N18
J2.83		isi.D[6]	2		SOC.P20
J2.72		isi.D[6]	6	Runs @ 1.8V.	SOC.AA3
J2.65		isi.D[7]	6	Runs @ 1.8V.	SOC.AA4
J2.77		isi.D[7]	2		SOC.P21
J2.46		isi.D[8]	2		SOC.R20
J2.69		isi.D[8]	6	Runs @ 1.8V.	SOC.Y5
J2.66		isi.D[9]	6	Runs @ 1.8V.	SOC.AA5
J2.40		isi.D[9]	2		SOC.R18
J3.38		isi.FRAME_VALID	2		SOC.K20
J2.73		isi.FRAME_VALID	6	Runs @ 1.8V.	SOC.T10
J3.58		isi.LINE_VALID	2		SOC.K21
J2.78		isi.LINE_VALID	6	Runs @ 1.8V. Internal buffer connected to this pin. It drives BOOT_MODE0, latched with POR_B rise.	SOC.V8
J3.30		isi.PCLK	2		SOC.J21

8.3 Ethernet Interface

The i.MX 91 SOC implements Two Ethernet controllers capable of simultaneous operation.
One 1G-bit Ethernet with AVB support (ENET) plus a separate 1Gbit Ethernet QoS with TSN support.

ENET_QOS (Ethernet Quality of Service) - Gigabit Ethernet controller based on Synopsys Proprietary with support for TSN (time-sensitive networking) in addition to EEE, Ethernet AVB, and IEEE 1588

ENET1 - Gigabit Ethernet controller with support for Energy Efficient Ethernet (EEE), Ethernet AVB (Audio Video Bridging, IEEE 802.1Qav), and IEEE 1588 time-stamping module which provides accurate clock synchronization for distributed control nodes for industrial automation applications.

8.3.1ENET_QOS (Ethernet Quality of Service)

The SOM can be ordered in one of the following configurations:

- **"EC" configuration** – The DART-MX91 includes an on SOM a Gigabit PHY (MaxLinear MxL86110) connected to ENET_QOS RGMII interface signals. External connectors and magnetics should be implemented on the carrier board to complete the interface to the media.
- **"no EC" configuration** – The DART-MX91 exposes the ENET_QOS RGMII/RMII interface signals to the SO-DIMM connector and ENET_QOS pins are referenced to 1.8V.

8.3.1.1 Ethernet PHY

The SOM MaxLinear MxL86110x Gigabit PHY, in conjunction with external magnetics on the carrier board, completes the interface to the media.
The following external gigabit magnetics are required to complete the Ethernet PHY interface for the media.

Table 7: Gigabit Ethernet Magnetics

Vendor	P/N	Package	Cores	Configuration
Pulse	H5007NL	Transformer	8	Auto-MDX
TDK	TLA-7T101LF	Transformer	8	Auto-MDX
Pulse	J0G-0009NL	Integrated RJ45	8	Auto-MDX

Table 8: Ethernet PHY Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
J1.2	EC	ETH0_MDI_B_P	0	Differential Pair Positive side	MxL86110x.4
J1.4	EC	ETH0_MDI_B_M	0	Differential Pair Negative side	MxL86110x.5
J1.6	EC	ETH0_MDI_A_M	0	Differential Pair Negative side	MxL86110x.2
J1.7	EC	ETH0_LED_LINK	0	Runs @ 3.3V. Active High.	MxL86110x.33
J1.8	EC	ETH0_MDI_A_P	0	Differential Pair Positive side	MxL86110x.1
J1.9	EC	ETH0_LED_ACT	0	Runs @ 3.3V. Active High.	MxL86110x.34
J1.10	EC	ETH0_MDI_C_P	0	Differential Pair Positive side	MxL86110x.6
J1.12	EC	ETH0_MDI_C_M	0	Differential Pair Negative side	MxL86110x.7
J1.14	EC	ETH0_MDI_D_P	0	Differential Pair Positive side	MxL86110x.9
J1.16	EC	ETH0_MDI_D_M	0	Differential Pair Negative side	MxL86110x.10
J2.82	EC	ETH_INT	0	Runs @ 1.8V.	MxL86110x.31

Table 9: MxL86110x Ethernet PHY LED Behavior

Symbol	10M link	10M active	100M link	100M active	1000M link	1000M active
LED_10_100_1000	ON	ON	ON	ON	ON	ON
LED_ACT	OFF	BLINK	OFF	BLINK	OFF	BLINK
ON = active; OFF = inactive						

8.3.1.2 ENET_QOS Signals

Table 10: ENET_QOS RMII/RGMII Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
J1.74		enet_qos.1588_EVENT0_IN	1	Will change level according to J1.90 NVCC_SD.	SOC.Y17
J1.82		enet_qos.1588_EVENT0_OUT	1	Will change level according to J1.90 NVCC_SD.	SOC.AA19
J1.13		enet_qos.MDC	0	Runs @ 3.3V. Routed through PMIC internal voltage translator. Has an internal 1.47K pull up.	SOC.AA11
J1.11		enet_qos.MDIO	0	Runs @ 3.3V. Routed through PMIC internal voltage translator. Has an internal 1.47K pull up.	SOC.AA10
J1.10	Non-EC	enet_qos.RGMII_RD0	0	Runs @ 1.8V.	SOC.AA8
J1.12	Non-EC	enet_qos.RGMII_RD1	0	Runs @ 1.8V.	SOC.Y9
J1.14	Non-EC	enet_qos.RGMII_RD2	0	Runs @ 1.8V.	SOC.AA9
J1.16	Non-EC	enet_qos.RGMII_RD3	0	Runs @ 1.8V.	SOC.Y10
J1.9	Non-EC	enet_qos.RGMII_RX_CTL	0	Runs @ 1.8V.	SOC.Y8
J1.7	Non-EC	enet_qos.RGMII_RXC	0	Runs @ 1.8V. Has EMI filter.	SOC.AA7
J1.4	Non-EC	enet_qos.RGMII_TD0	0	Runs @ 1.8V.	SOC.W11
J1.2	Non-EC	enet_qos.RGMII_TD1	0	Runs @ 1.8V.	SOC.T12
J1.6	Non-EC	enet_qos.RGMII_TD2	0	Runs @ 1.8V.	SOC.U12
J1.8	Non-EC	enet_qos.RGMII_TD3	0	Runs @ 1.8V.	SOC.V12
J1.3	Non-EC	enet_qos.RGMII_TX_CTL	0	Runs @ 1.8V.	SOC.V10
J1.5	Non-EC	enet_qos.RGMII_TXC	0	Runs @ 1.8V.	SOC.U10
J1.7	Non-EC	enet_qos.RX_ER	1	Runs @ 1.8V. Has EMI filter.	SOC.AA7
J1.5	Non-EC	enet_qos.TX_ER	1	Runs @ 1.8V.	SOC.U10
J1.6	Non-EC	INPUT=enet_qos.TX_CLK OUTPUT=ENET_CLK_ROOT	1	Runs @ 1.8V.	SOC.U12

8.3.2ENET2

ENET2 RGMII/RMII interface signals are always exported through SO-DIMM connector.
Signals, in conjunction to MDIO signals exported from SO-DIMM connector, they can be used to interface an external Ethernet PHY.

ENET2 pins are referenced to 1.8V.

8.3.2.1 ENET2 Signals

Table 11: ENET2 RMII/RGMII Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
J1.88		enet2.1588_EVENT0_IN	1	Will change level according to J1.90 NVCC_SD.	SOC.Y19
J1.86		enet2.1588_EVENT0_OUT	1	Will change level according to J1.90 NVCC_SD.	SOC.Y18
J1.80		enet2.1588_EVENT1_IN	1	Will change level according to J1.90 NVCC_SD.	SOC.AA18
J1.78		enet2.1588_EVENT1_OUT	1	Will change level according to J1.90 NVCC_SD.	SOC.Y20
J2.27	SDEX	enet2.MDIO	0	Runs @ 1.8V.	SOC.AA6
J2.65		enet2.RGMII_RD0	0	Runs @ 1.8V.	SOC.AA4
J2.69		enet2.RGMII_RD1	0	Runs @ 1.8V.	SOC.Y5
J2.66		enet2.RGMII_RD2	0	Runs @ 1.8V.	SOC.AA5
J2.68		enet2.RGMII_RD3	0	Runs @ 1.8V.	SOC.Y6
J2.64		enet2.RGMII_RX_CTL	0	Runs @ 1.8V.	SOC.Y4
J2.72		enet2.RGMII_RXC	0	Runs @ 1.8V.	SOC.AA3
J2.70		enet2.RGMII_TD0	0	Runs @ 1.8V.	SOC.T8
J2.67		enet2.RGMII_TD1	0	Runs @ 1.8V.	SOC.U8
J2.78		enet2.RGMII_TD2	0	Runs @ 1.8V. The internal buffer connected to this pin drives BOOT_MODE0 (J2.90), latched with POR_B rise.	SOC.V8
J2.73		enet2.RGMII_TD3	0	Runs @ 1.8V.	SOC.T10
J2.74		enet2.RGMII_TX_CTL	0	Runs @ 1.8V.	SOC.V6
J2.71		enet2.RGMII_TXC	0	Runs @ 1.8V.	SOC.U6
J2.72		enet2.RX_ER	1	Runs @ 1.8V.	SOC.AA3
J2.71		enet2.TX_ER	1	Runs @ 1.8V.	SOC.U6
J2.78		IN=enet2.TX_CLK OUT=ENET_REF_CLK_ROOT	1	Runs @ 1.8V. The internal buffer connected to this pin drives BOOT_MODE0 (J2.90), latched with POR_B rise.	SOC.V8

8.4 Wi-Fi, BT, 802.15.4

The DART-MX91 contains a certified high-performance Wi-Fi, Bluetooth, 802.15.4 module:

- Wi-Fi® 802.11a/b/g/n/ac/ax
- Bluetooth® 5.4 BR/EDR/LE
- 802.15.4
- Modules have an antenna connection through a 50Ω U. FL JACK connector

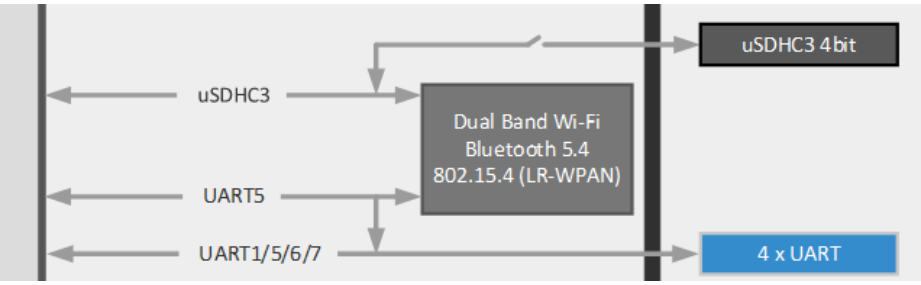


Figure 3: DART-MX91 Wi-Fi Module Internal Connection

8.4.1Interface Implementation Options

8.4.1.1 Module Configuration with "WBD" Option

- System use: **Wi-Fi and Bluetooth**.
  - BT UART external interface pins should be left floating.
- System use: **Wi-Fi and no BT**.
  - In this case, disable the BT module (using GPIO4.IO[15]).
  - BT UART interface pins can be used externally with any of the alternate functions.
- System use: **BT and no Wi-Fi.**
  - Disable Wi-Fi function.
  - Enable the BT module (using GPIO4.IO[15]).

8.4.1.2 Module Configuration with "WBE" Option

- System use: **Wi-Fi and Bluetooth and 802.15.4**.
  - BT UART external interface pins should be left floating.
  - TP SPI pins can be used in SPI mode only
- System use: **Wi-Fi and no BT no 802.15.4**.
  - In this case, disable the BT and 802.15.4 module (using GPIO4.IO[15]).
  - BT UART and TP SPI interface pins can be used externally with any of the alternate functions.
- System use: **BT and 802.15.4 and no Wi-Fi.**
  - Disable Wi-Fi function.
  - Enable the BT and 802.15.4 module (using GPIO4.IO[15]).

8.4.1.3 Module Configuration without "WBD" or "WBE" Option

- System use: **no Wi-Fi and no BT**.
  - BT UART interface accessible externally with any of its alternative functions.
  - SD3 interface accessible externally with any of its alternative functions.
    SD3 is working at 1.8V levels

8.4.2Bluetooth Interface Signals

Table 12: BT UART Interface Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
J2.26		uart5.CTS_B	6	Runs @ 1.8V. Used internally with "WBD" or “WBE” Function can be released if BT Function disabled Always exposed	SOC.Y1
J2.22		uart5.RTS_B	6	Runs @ 1.8V. Used internally with "WBD" or “WBE” Function can be released if BT Function disabled Always exposed	SOC.W2
J2.24		uart5.RX	6	Runs @ 1.8V. Used internally with "WBD" or “WBE” Function can be released if BT Function disabled Always exposed	SOC.W1
J2.20		uart5.TX	6	Runs @ 1.8V. Used internally with "WBD" or “WBE” Function can be released if BT Function disabled Always exposed	SOC.Y2

8.4.3Wakeup signals

The DART-MX91 exposes Wi-Fi and BT wakeup signals of the modules on the SOM. The voltage levels of the signals are 1.8V.
The purpose of these signals is to be connected externally to some GPIO lines and use as a wakeup source for the main CPU.
For implementation, please check out the Wi-Fi module datasheet.

Table 13: Wakeup Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
J1.25	WBD/WBE	WIFI_HOST_WAKE		Runs @ 1.8V.	LBES5PL2xL.73
J1.32	WBD/WBE	BT_DEV_WAKE		Runs @ 1.8V.	LBES5PL2xL.75
J1.23	WBD/WBE	BT_HOST_WAKE		Runs @ 1.8V.	LBES5PL2xL.76

8.5 Ultra-Secured Digital Host Controller

The DART-MX91 exposes the uSDHC2 controller 4-bit interface for supporting interface between the host system and the SD/SDIO/MMC cards.
Key features of uSDHC2:

- SD/SDIO standard, up to version 3.0.
- compliance with 200 MHz SDR signaling to support up to 100 MB/sec
- 1.8 V and 3.3 V operation
- Support for SDXC (extended capacity)

8.5.1uSDHC1 Signals

uSDHC controller, uSDHC1, is used internally for the eMMC storage chip on the SOM.

8.5.2uSDHC2 Signals

uSDHC2 pins are referenced to LDO5 power supply of the PMIC.
By default, this LDO supplies 3.3V to allow proper boot from SD Card.
The system uses SD2_VSELECT pin to switch between 3.3V and 1.8V.
This pin functionality can be changed to GPIO3.IO[19] and controlled programmatically.
It is also possible to control the voltage of the LDO by I2C commands.

- Low state will select 3.3V interface
- High state will select 1.8V interface

Table 14: uSDHC2 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
J1.74		usdhc2.CD_B	0	External SD card detect input. Add 10K external pull up to J1.90. Will change level according to J1.90 NVCC_SD.	SOC.Y17
J1.82		usdhc2.CLK	0	Will change level according to J1.90 NVCC_SD.	SOC.AA19
J1.88		usdhc2.CMD	0	Will change level according to J1.90 NVCC_SD.	SOC.Y19
J1.86		usdhc2.DATA0	0	Will change level according to J1.90 NVCC_SD.	SOC.Y18
J1.80		usdhc2.DATA1	0	Will change level according to J1.90 NVCC_SD.	SOC.AA18
J1.78		usdhc2.DATA2	0	Will change level according to J1.90 NVCC_SD.	SOC.Y20
J1.84		usdhc2.DATA3	0	Will change level according to J1.90 NVCC_SD.	SOC.AA20
J2.25	SDEX	usdhc2.RESET_B	0	Runs @ J1.90 VDD_SDIO2 level.	SOC.AA17

8.5.3uSDHC3 Signals

The uSDHC3 controller serves as the internal interface for Wi-Fi connectivity on the System on Module (SOM). It can be utilized in scenarios where the Wi-Fi module is not installed, through two distinct pin configurations. One configuration operates at a voltage level of 3.3V, while the alternative operates at 1.8V. The 3.3V pin group is consistently accessible; however, it is important to note that the uSDHC3 functionality cannot be employed simultaneously with the Wi-Fi interface. The 1.8V pin group is only available on SOMs that do not have the Wi-Fi module integrated.

Table 15: uSDHC3 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
J2.45	SDEX	usdhc3.CLK	0	Runs @ 1.8V.	SOC.V16
J3.42		usdhc3.CLK	1	Runs @ 3.3V. Cannot be used if the Wi-Fi module is active.	SOC.U18
J2.43	SDEX	usdhc3.CMD	0	Runs @ 1.8V.	SOC.U16
J3.46		usdhc3.CMD	1	Runs @ 3.3V. Cannot be used if the Wi-Fi module is active.	SOC.U20
J2.35	SDEX	usdhc3.DATA0	0	Runs @ 1.8V.	SOC.T16
J3.64		usdhc3.DATA0	1	Runs @ 3.3V. Cannot be used if the Wi-Fi module is active.	SOC.U21
J2.33	SDEX	usdhc3.DATA1	0	Runs @ 1.8V.	SOC.V14
J2.60		usdhc3.DATA1	1	Runs @ 3.3V. Cannot be used if the Wi-Fi module is active.	SOC.V21
J2.31	SDEX	usdhc3.DATA2	0	Runs @ 1.8V.	SOC.U14
J2.42		usdhc3.DATA2	1	Runs @ 3.3V. Cannot be used if the Wi-Fi module is active.	SOC.V20
J2.29	SDEX	usdhc3.DATA3	0	Runs @ 1.8V.	SOC.T14
J2.54		usdhc3.DATA3	1	Runs @ 3.3V. Cannot be used if the Wi-Fi module is active.	SOC.W21

8.6 USB 2.0

The DART-MX91 features dual USB controllers and PHYs that are compliant with USB 2.0 standards.

8.6.1USB Port1 Interface Signals

Table 16: USB 3.0/2.0 Port 1 Interface signals

Pin#	Assy	Pin Function	Alt #	Notes	Ball
J1.13		usb1.OTG_ID	3	Runs @ 3.3V. Routed through PMIC internal voltage translator. It has an internal 1.47K pull-up. **It is not recommended to use a native USB_ID.** **General GPIO usage is recommended.**	SOC.AA11
J1.2	Non-EC	usb1.OTG_OC	3	Runs @ 1.8V.	SOC.T12
J1.11		usb1.OTG_PWR	3	Runs @ 3.3V. Routed through PMIC internal voltage translator. Has an internal 1.47K pull up.	SOC.AA10
J3.67		USB1_D_N	0	Differential Pair Negative side	SOC.A14
J3.65		USB1_D_P	0	Differential Pair Positive side	SOC.B14
J3.56		USB1_ID	0	Runs @ 1.8V. USB1 native ID analogue input. No GPIO function. **It is not recommended to use a native USB_ID.** **General GPIO usage is recommended.**	SOC.C11
J3.66		USB1_VBUS	0	Runs @ 5.0V. VBUS detect input.	SOC.F12

Note: *Usage of native USB_ID in i.MX91 requires patches not included in NXP formal release.*
For simple OTG implementation, use a CC Logic chip and connect to GPIO.
See the EVK schematics for reference. USB1_ID can be left floating if not used.

8.6.2USB Port2 Interface Signals

Table 17: USB 2.0 Port 2 Interface signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
J1.8	Non-EC	usb2.OTG_ID	3	Runs @ 1.8V. **It is not recommended to use a native USB_ID.** **General GPIO usage is recommended.**	SOC.V12
J1.6	Non-EC	usb2.OTG_OC	3	Runs @ 1.8V.	SOC.U12
J1.9	Non-EC	usb2.OTG_PWR	3	Runs @ 1.8V.	SOC.Y8
J3.49		USB2_D_N	0		SOC.A15
J3.47		USB2_D_P	0		SOC.B15
J3.44		USB2_ID	0	Runs @ 1.8V. USB2 native ID analogue input. No GPIO function. **It is not recommended to use a native USB_ID.** **General GPIO usage is recommended.**	SOC.E12
J3.26		USB2_VBUS	0	Runs @ 5.0V. VBUS detect input.	SOC.E14

Note: *Usage of native USB_ID in i.MX91 requires patches not included in NXP formal release.*
For simple OTG implementation, use a CC Logic chip and connect to GPIO.
See the EVK schematics for reference. USB1_ID can be left floating if not used.

8.7 Audio

The DART-MX91 features the following audio interfaces:

- WM8904CGEFL Audio codec interfaces:
  - Analog outputs & inputs: stereo line-in & Stereo HP out.
  - Digital microphone input
- Five external SAI (synchronous audio interface) modules supporting I2S, AC97, TDM, codec/DSP and DSD interfaces:
  - SAI-1 supports to up to 16-channels TX (8 lanes) and 16-channels RX (8 lanes) at 768KHz/32-bit
  - SAI-2/5 supports to up to 8-channels TX (4 lanes) and 8-channels RX (4 lanes) at 768KHz/32-bit
  - SAI-3 supports up to 4-channels TX (2 lanes) and 4-channels RX (2 lanes) at 768KHz/32-bit
  - SAI-6 supports to up to 2-channels TX (1 lanes) and 2-channels RX (1 lanes) at 768KHz/32-bit when multiplexed on SAI1, or up to 384kHz/32-bit when multiplexed on Ethernet primary pins
  - SAI-7 supports to up to 2-channels TX (1 lanes) and 2-channels RX (1 lanes) at 384KHz/32-bit
- PDM supporting up to 8-channels (4 lanes)
- S/PDIF Input and Output, including a new Raw Capture input mode
- Hifi4 Audio DSP, operating up to 800 MHz

Analog audio signals are part of the SOM WM8904 audio codec, available with **"AC" Configuration** only. The codec interfaces the SoC via SAI3 lines, when not assembled, SoC balls are exported to SOM connector instead of Analog codec interface pins.

The Codec features stereo ground-referenced headphone amplifiers using the Wolfson 'Class-W' amplifier techniques -incorporating an innovative dual-mode charge pump architecture - to optimize efficiency and power consumption during playback. The ground-referenced headphone and line outputs eliminate AC coupling capacitors, and both outputs include common mode feedback paths to reject ground noise.

The following figure illustrates the connectivity for no large AC coupling capacitors implemented on SOM.

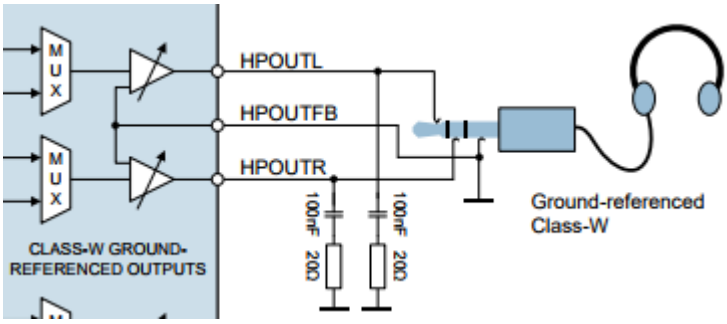


Figure 4: WM8904 Headphone connectivity

8.7.1WM8904CGEFL Audio Codec

8.7.1.1 Audio Codec Signals

Table 18: Analog audio Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
J2.12		AGND	0		
J2.2	AC	HPLOUT	0	100nF and 20Ω Zobel network required.	WM8904.13
J2.6	AC	HPOUTFB	0	Headphone output ground loop noise rejection feedback. Should be connected to GND near the HP Connector.	WM8904.14
J2.4	AC	HPROUT	0	100nF and 20Ω Zobel network required.	WM8904.15
J2.14	AC	DMIC_CLK	0	DMIC output.	WM8904.1
J2.16	AC	DMIC_DATA	0	Runs @ 1.8V. DMIC input.	WM8904.27
J2.8	AC	LINEIN1_LP	0		WM8904.26
J2.10	AC	LINEIN1_RP	0		WM8904.24

8.7.2Serial Audio Interface

The SAI module provides a synchronous audio interface that supports full duplex serial interfaces with frame synchronization, such as I2S, AC97, TDM, and codec/DSP interfaces.

8.7.2.1 SAI Signals

Table 19: Serial Audio Interface Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
J2.2	Non-AC	sai1.MCLK	1		SOC.H20
J2.14	Non-AC	sai1.MCLK	6	BOOT_MODE3 pin. Has an internal SOC PD. Do not drive until after POR_B rise + 30ms.	SOC.H21
J2.16	Non-AC	sai1.MCLK	4		SOC.F20
J2.8	Non-AC	sai1.RX_BCLK	4		SOC.D21
J2.2	Non-AC	sai1.RX_DATA[0]	0		SOC.H20
J2.6	Non-AC	sai1.RX_SYNC	4		SOC.D20
J2.4	Non-AC	sai1.TX_BCLK	0		SOC.G20
J2.14	Non-AC	sai1.TX_DATA[0]	0	BOOT_MODE3 pin. Has an internal SOC PD. Do not drive until after POR_B rise + 30ms.	SOC.H21
J2.10	Non-AC	sai1.TX_DATA[1]	1	BOOT_MODE2 pin. Has an internal SOC PD. Do not drive until after POR_B rise + 30ms	SOC.G21
J2.10	Non-AC	sai1.TX_SYNC	0	BOOT_MODE2 pin. Has an internal SOC PD. Do not drive until after POR_B rise + 30ms	SOC.G21
J2.66		sai2.MCLK	2	Runs @ 1.8V.	SOC.AA5
J2.27	SDEX	sai2.RX_BCLK	2	Runs @ 1.8V.	SOC.AA6
J2.73		sai2.RX_DATA[0]	2	Runs @ 1.8V.	SOC.T10
J2.71		sai2.TX_BCLK	2	Runs @ 1.8V.	SOC.U6
J2.64		sai2.TX_DATA[0]	2	Runs @ 1.8V.	SOC.Y4
J2.74		sai2.TX_SYNC	2	Runs @ 1.8V.	SOC.V6
J2.46		sai3.MCLK	1		SOC.R20
J2.40		sai3.RX_BCLK	1		SOC.R18
J2.44		sai3.RX_BCLK	7		SOC.T21
J2.36		sai3.RX_DATA[0]	1		SOC.T20
J2.34		sai3.RX_SYNC	1		SOC.R17
J2.79		sai3.RX_SYNC	7		SOC.N20
J2.38		sai3.TX_BCLK	1		SOC.R21
J2.44		sai3.TX_DATA[0]	1		SOC.T21
J2.34		sai3.TX_DATA[0]	7		SOC.R17
J1.74		sai3.TX_SYNC	7	External SD card detect input. Will change level according to J1.90 NVCC_SD.	SOC.Y17
J2.42		sai3.TX_SYNC	7		SOC.V20

8.7.3PDM - Microphone Interface (MICFIL)

The PDM module of the i.MX91 SOC, provides a popular way to deliver audio from microphones to the processor in several applications, such as mobile telephones.
Up to 8 channels can be implemented with 4 lanes.

The PDM Microphone Interface module is composed of:

- A decimation filter by channel that:
  - Consists, internally, of a cascade integrator comb (CIC) filter, a DC remover, and half-band filters. The filtering results are stored in individual FIFOs (a FIFO per channel). These FIFOs have overflow and underflow detectors to deliver an error interrupt request.
  - Implements a low-pass filter in the audio band (20 Hz–20.0 kHz @48 kHz output sampling rate by default) with a configurable decimation rate. You can implement it using a series of CIC, half-band, and DC remover filters.
  - Stores its output into a FIFO buffer, and each FIFO is mapped to MICFIL Output Result (DATACH0 - DATACH7). It is possible to generate either an interrupt or a DMA request when, in each FIFO of all enabled channels, the number of data stored surpasses a configured watermark.
  - Independently on decimation filters, there is a Hardware Voice Activity Detector (HWVAD) which implements voice-detection algorithms to generate wake-up interrupts.
- A shared time generator unit that:
  - Delivers the PDM_CLK to all microphones that must operate at the same clock frequency. Each input interface receives a time multiplexed PDM bitstream from two PDM microphones and it separates audio information in two channels: left (0) and right (1). Every decimation filter, corresponding to its channel, does this processing.
  - Generates the PDM_CLK to the microphones. This clock is the same and is active for all the PDM microphones, which means, it is not possible to turn off the PDM_CLK only for one single microphone.
- An input interface for each pair of PDM microphones
- A FIFO by channel
- A shared DMA interface, interrupt interface, and bus interface
- A shared interface to the chip
- A Hardware Voice Activity Detector (HWVAD)

PDM block main features are:

- Decimation filters:
  - Fixed-point filtering
  - 24-bit PCM audio output
  - Internal clock divider for a programmable PDM clock generation
- Full or partial set of channel operations with individual enable controls
- Programmable decimation rate
- Programmable DC remover
- Programmable DC remover at output
- Range adjustment capability
- FIFOs with interrupt and DMA capability: each FIFO having a length of 32 entries

- HWVAD, equipped with:
  - Interrupt capability
  - Zero-Crossing Detection (ZCD) option

Table 20: PDM Interface Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
J2.36		pdm.BIT_STREAM[0]	2		SOC.T20
J2.56		pdm.BIT_STREAM[0]	0		SOC.J17
J2.85		pdm.BIT_STREAM[0]	2		SOC.L18
J1.19		pdm.BIT_STREAM[1]	2		SOC.L20
J2.42		pdm.BIT_STREAM[1]	2		SOC.V20
J3.62		pdm.BIT_STREAM[1]	0		SOC.G18
J2.38		pdm.BIT_STREAM[2]	2		SOC.R21
J2.79		pdm.BIT_STREAM[2]	2		SOC.N20
J2.34		pdm.BIT_STREAM[3]	2		SOC.R17
J2.81		pdm.BIT_STREAM[3]	2		SOC.N21
J2.44		pdm.CLK	2		SOC.T21
J2.50		pdm.CLK	0		SOC.G17
J2.86		pdm.CLK	2		SOC.L17

8.7.4MQS - Medium Quality Sound

Medium-quality sound (MQS) is used to generate medium-quality audio via a standard GPIO in the pin mux, allowing the user to connect stereo speakers or headphones to a power amplifier without an additional DAC chip.

Table 21: MQS Interface Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
J2.10		mqs1.LEFT	4	BOOT_MODE2 pin. Has an internal SOC PD. Do not drive until after POR_B rise + 30ms	SOC.G21
J2.50		mqs1.LEFT	1		SOC.G17
J2.2	Non-AC	mqs1.RIGHT	4		SOC.H20
J2.56		mqs1.RIGHT	1		SOC.J17
J1.84		mqs2.LEFT	2	Will change level according to J1.90 NVCC_SD.	SOC.AA20
J2.24		mqs2.LEFT	1	Runs @ 1.8V. Used on DART for BT communication. If BT not required internal buffer can be disabled, and pin function released to customer usage.	SOC.W1
J2.68		mqs2.LEFT	3	Runs @ 1.8V.	SOC.Y6
J1.78		mqs2.RIGHT	2	Will change level according to J1.90 NVCC_SD.	SOC.Y20
J2.20		mqs2.RIGHT	1	Runs @ 1.8V. Used on DART for BT communication. If BT not required internal buffer can be disabled, and pin function released to customer usage.	SOC.Y2
J2.66		mqs2.RIGHT	3	Runs @ 1.8V.	SOC.AA5

8.7.5SPDIF – Sony Philips Digital Interface Format

A standard audio file transfer format, developed jointly by the Sony and Phillips corporations. It supports Transmitter and Receiver functionality including frequency measurement block that allows the precise measurement of an incoming sampling frequency.
The SPDIF receiver extracts the audio data from each SPDIF frame and places the data in the SPDIF Rx left and right FIFOs with Channel Status and User bits.
For the SPDIF transmitter, the audio data is provided by the processor dedicated registers along with Channel Status and User bits.

Table 22: SPDIF Interface Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
J2.68		spdif1.IN	2	Runs @ 1.8V.	SOC.Y6
J2.69		spdif1.IN	1	Runs @ 1.8V.	SOC.Y5
J3.42		spdif1.IN	2		SOC.U18
J2.68		spdif1.OUT	1	Runs @ 1.8V.	SOC.Y6
J3.46		spdif1.OUT	2		SOC.U20

8.8 LPUART

The DART-MX91 exposes up to seven LPUART interfaces some of which are multiplexed with other peripherals. UART5 is used on SOM for Bluetooth interface and can be accessible only if the BT is disabled or on SOM without ***"WBD" and "WBE" Configuration***.

The LPUART includes the following features:

- Full-duplex, standard NRZ format
- Programmable baud rates (13-bit modulo divider) with a configurable oversampling ratio (OSR)
- Asynchronous operations of transmit and receive baud rates with respect to the bus clock:
    - Baud rate can be configured independently of the bus clock frequency.
    - Operation in Low-Power modes is supported.
- Interrupt, DMA, or polled operations:
    - Transmit data empty and transmission complete
    - Receive data full
    - Receive overrun, parity error, framing error, and noise error
    - Idle receiver detect
    - Active edge on receive pin
    - Break detect supporting LIN
    - Receive data match
- Hardware parity generation and checking
- Programmable 7-bit, 8-bit, 9-bit, or 10-bit character length
- Programmable 1-bit or 2-bit stop bits
- Support for three receiver wakeup methods:
    - Idle line wakeup
    - Address mark wakeup
    - Receive data match
- Automatic address matching to reduce ISR overhead:
    - Address mark matching
    - Idle line address matching
    - Address match start, address match end
- Optional 13-bit and 11-bit break character generation
- Configurable idle length detection supporting 1, 2, 4, 8, 16, 32, 64, or 128 idle characters
- Selectable transmitter output and receiver input polarity
- Hardware flow control support for request to send (RTS) and clear to send (CTS) signals
- Selectable IrDA 1.4 return-to-zero-inverted (RZI) format with a programmable pulse width
- Independent FIFO structure for transmit and receive functions:
    - Separate configurable watermarks for receive and transmit requests
    - Option for receiver to assert request after a configurable number of idle characters, if receive FIFO is not empty

Unlike other i.MX8M based SOMs the direction of the UART lines cannot be programmed. The following table shows the direction of signals of i.MX91 LPUARTs

Table 23: LPUART I/O Direction

Signal	Direction
uartX.TX	Output
uartX.RX	Input
uartX.RTS_B	Output
uartX.CTS_B	Input

8.8.1LPUART1 Signals

Table 24: LPUART1 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
J2.45	SDEX	uart1.CTS_B	2	Runs @ 1.8V	SOC.V16
J2.16	Non-AC	uart1.CTS_B	1		SOC.F20
J2.32		uart1.DCD_B	2		SOC.C20
J2.4	Non-AC	uart1.DSR_B	3		SOC.G20
J2.14	Non-AC	uart1.DTR_B	3	BOOT_MODE3 pin. Has an internal SOC PD. Do not drive until after POR_B rise + 30ms	SOC.H21
J2.30		uart1.RIN_B	2		SOC.C21
J2.43	SDEX	uart1.RTS_B	2	Runs @ 1.8V	SOC.U16
J1.80		uart1.RX	3	Will change level according to J1.90 NVCC_SD	SOC.AA18
J2.88		uart1.RX	0	Used as console debug on Variscite release	SOC.E20
J2.90		uart1.TX	0	Used as console debug on Variscite release. BOOT_MODE0 pin. Do not drive until after POR_B rise + 30ms. Internal buffer connected to J2. 78 drives this pin	SOC.E21
J1.86		uart1.TX	3	Will change level according to J1.90 NVCC_SD	SOC.Y18

8.8.2LPUART2 Signals

Table 25: LPUART2 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
J2.4	Non-AC	uart2.CTS_B	1		SOC.G20
J2.35	SDEX	uart2.CTS_B	2	Runs @ 1.8V	SOC.T16
J2.6	Non-AC	uart2.DCD_B	2		SOC.D20
J2.2	Non-AC	uart2.DSR_B	3		SOC.H20
J2.10	Non-AC	uart2.DTR_B	3	BOOT_MODE2 pin. Has an internal SOC PD. Do not drive until after POR_B rise + 30ms	SOC.G21
J2.8	Non-AC	uart2.RIN_B	2		SOC.D21

Pin#	Assy	Pin Function	Alt#	Notes	Ball
J2.14	Non-AC	uart2.RTS_B	1	BOOT_MODE3 pin. Has an internal SOC PD. Do not drive until after POR_B rise + 30ms	SOC.H21
J2.33	SDEX	uart2.RTS_B	2	Runs @ 1.8V	SOC.V14
J1.84		uart2.RX	3	Will change level according to J1.90 NVCC_SD	SOC.AA20
J2.16	Non-AC	uart2.RX	0		SOC.F20
J1.78		uart2.TX	3	Will change level according to J1.90 NVCC_SD	SOC.Y20

8.8.3LPUART3 Signals

Table 26: LPUART3 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
J2.38		uart3.CTS_B	4		SOC.R21
J1.12	Non-EC	uart3.CTS_B	1	Runs @ 1.8V	SOC.Y9
J1.13		uart3.DCD_B	1	Runs @ 3.3V. Routed through PMIC internal voltage translator. Has an internal 1.47K pull up	SOC.AA11
J1.9	Non-EC	uart3.DSR_B	1	Runs @ 1.8V	SOC.Y8
J1.3	Non-EC	uart3.DTR_B	1	Runs @ 1.8V	SOC.V10
J1.11		uart3.RIN_B	1	Runs @ 3.3V. Routed through PMIC internal voltage translator. Has an internal 1.47K pull up	SOC.AA10
J2.46		uart3.RTS_B	4		SOC.R20
J1.2	Non-EC	uart3.RTS_B	1	Runs @ 1.8V	SOC.T12
J1.10	Non-EC	uart3.RX	1	Runs @ 1.8V	SOC.AA8
J2.77		uart3.RX	1		SOC.P21
J1.4	Non-EC	uart3.TX	1	Runs @ 1.8V	SOC.W11
J2.83		uart3.TX	1		SOC.P20

8.8.4LPUART4 Signals

Table 27: LPUART4 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
J2.66		uart4.CTS_B	1	Runs @ 1.8V	SOC.AA5
J2.38		uart4.CTS_B	6		SOC.R21
J2.64		uart4.DSR_B	1	Runs @ 1.8V	SOC.Y4
J2.74		uart4.DTR_B	1	Runs @ 1.8V	SOC.V6
J2.27	SDEX	uart4.RIN_B	1	Runs @ 1.8V	SOC.AA6
J2.67		uart4.RTS_B	1	Runs @ 1.8V	SOC.U8
J2.46		uart4.RTS_B	6		SOC.R20
J2.77		uart4.RX	6		SOC.P21
J2.65		uart4.RX	1	Runs @ 1.8V	SOC.AA4

Pin#	Assy	Pin Function	Alt#	Notes	Ball
J2.83		uart4.TX	6		SOC.P20
J2.70		uart4.TX	1	Runs @ 1.8V	SOC.T8

8.8.5LPUART5 Signals

Table 28: LPUART5 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
J3.38		uart5.CTS_B	5	Pin can be used as UART5 when BT disabled	SOC.K20
J2.26		uart5.CTS_B	6	Runs @ 1.8V. Used on DART for BT communication. Pin can be used when BT disabled	SOC.Y1
J2.22		uart5.RTS_B	6	Runs @ 1.8V. Used on DART for BT communication. Pin can be used when BT disabled	SOC.W2
J3.58		uart5.RTS_B	5	Pin can be used as UART5 when BT disabled	SOC.K21
J2.24		uart5.RX	6	Runs @ 1.8V. Used on DART for BT communication. Pin can be used when BT disabled	SOC.W1
J3.50		uart5.RX	5	Pin can be used as UART5 when BT disabled	SOC.J20
J2.20		uart5.TX	6	Runs @ 1.8V. Used on DART for BT communication. Pin can be used when BT disabled	SOC.Y2
J3.30		uart5.TX	5	Pin can be used as UART5 when BT disabled	SOC.J21

8.8.6LPUART6 Signals

Table 29: LPUART6 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
J1.19		uart6.CTS_B	5		SOC.L20
J1.17		uart6.RTS_B	5		SOC.L21
J2.85		uart6.RX	5		SOC.L18
J2.86		uart6.TX	5		SOC.L17

8.8.7LPUART7 Signals

Table 30: LPUART7 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
J2.48		uart7.CTS_B	5		SOC.N17
J2.80		uart7.RTS_B	5		SOC.N18
J2.87		uart7.RX	5		SOC.M21
J2.89		uart7.TX	5		SOC.M20

8.8.8LPUART8 Signals

Table 31: LPUART8 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
J2.83		uart8.CTS_B	5		SOC.P20
J2.77		uart8.RTS_B	5		SOC.P21
J2.81		uart8.RX	5		SOC.N21
J2.79		uart8.TX	5		SOC.N20

8.9 Flexible Controller Area Network

The FlexCAN module is a communication controller implementing the CAN protocol according to the ISO 11898-1:2015 standard and CAN 2.0 B protocol specifications

Signal Description:

- CAN Rx: The receive pin from the CAN bus transceiver. Dominant state is represented by logic level '0'. Recessive state is represented by logic level '1'.
- CAN Tx: The transmit pin to the CAN bus transceiver. Dominant state is represented by logic level '0'. Recessive state is represented by logic level '1'.

8.9.1FLEXCAN1 Signals

Table 32: FLEXCAN1 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
J2.4	Non-AC	can1.RX	4		SOC.G20
J2.56		can1.RX	6		SOC.J17
J2.14	Non-AC	can1.TX	4	BOOT_MODE3 pin. Has an internal SOC PD. Do not drive until after POR_B rise + 30ms.	SOC.H21
J2.50		can1.TX	6		SOC.G17

8.9.2FLEXCAN2 Signals

Table 33: FLEXCAN2 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
J1.6	Non-EC	can2.RX	2	Runs @ 1.8V.	SOC.U12
J1.80		can2.RX	2	Will change level according to J1.90 NVCC_SD.	SOC.AA18
J2.20		can2.RX	3	Runs @ 1.8V. Used on DART for BT communication. If BT not required internal buffer can be disabled, and pin function released to customer usage.	SOC.Y2
J2.54		can2.RX	2		SOC.W21
J1.8	Non-EC	can2.TX	2	Runs @ 1.8V.	SOC.V12
J1.86		can2.TX	2	Will change level according to J1.90 NVCC_SD.	SOC.Y18
J2.24		can2.TX	3	Runs @ 1.8V. Used on DART for BT communication. If BT not required internal buffer can be disabled, and pin function released to customer usage.	SOC.W1
J2.60		can2.TX	2		SOC.V21

8.10 LPSPI - Low Power Serial Peripheral Interface

The DART-MX91 exposes up to 7 LPSPI interfaces.

LPSPI provides an efficient interface to a SPI bus, either as a master or slave. A SPI bus is a synchronous serial communication interface used in embedded systems. It is typically used to perform short distance communications between microcontrollers and peripheral devices, on printed circuit boards. Typical applications include interfacing to Secure Digital cards and LCD displays.

Key features of the ECSPI include:

- Requires minimal CPU overhead, with DMA offloading of FIFO register accesses
- Continues operating in Stop mode, if configured to do so and an appropriate clock is available
- Supports DMA accesses and generates DMA requests
- 32-bit word size
- Configurable clock polarity and phase
- Master mode—supports up to 2 peripheral chip selects
- Slave mode
- 8-word transmit and command FIFO
- 8-word receive FIFO
- Flexible timing parameters in Master mode, including SCK frequency and duty cycle, and delays between PCS and SCK edges
- Continuous transfer option to keep PCS asserted across multiple frames
- Full-duplex transfers support 1-bit transmit and receive on each clock edge
- Half-duplex transfers support:
    - 1-bit transmit or receive on each clock edge
- Receive data match logic supports discard of non-matching data and interrupt on data match

Note: *For interacting multiple peripherals on same SPI bus, one can define any GPIO to be used as chip select. Examples can be found in our DTS files.*

8.10.1 LPSPI1 Signals

Table 34: LPSPI1 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
J2.10		spi1.PCS0	2	BOOT_MODE2 pin. Has an internal SOC PD. Do not drive until after POR_B rise + 30ms	SOC.G21
J2.56		spi1.PCS1	2		SOC.J17
J2.14	Non-AC	spi1.SCK	2	BOOT_MODE3 pin. Has an internal SOC PD. Do not drive until after POR_B rise + 30ms.	SOC.H21
J2.4	Non-AC	spi1.SIN	2		SOC.G20
J2.2	Non-AC	spi1.SOUT	2		SOC.H20

8.10.2 LPSPI2 Signals

Table 35: LPSPI2 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
J2.90		spi2.PCS0	2	Used as console debug on Variscite release. BOOT_MODE0 pin. Do not drive until after POR_B rise + 30ms. Internal buffer connected to J2.78 drives this pin	SOC.E21
J1.9	Non-EC	spi2.PCS0	2	Runs @ 1.8V	SOC.Y8
J3.62		spi2.PCS1	2		SOC.G18
J1.3	Non-EC	spi2.SCK	2	Runs @ 1.8V	SOC.V10
J2.88		spi2.SIN	2	Used as console debug on Variscite release	SOC.E20
J1.5	Non-EC	spi2.SIN	2	Runs @ 1.8V	SOC.U10
J2.16	Non-AC	spi2.SOUT	2		SOC.F20
J1.7	Non-EC	spi2.SOUT	2	Runs @ 1.8V. Has EMI filter	SOC.AA7

8.10.3 LPSPI3 Signals

Table 36: LPSPI3 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
J2.89		spi3.PCS0	1		SOC.M20
J1.17		spi3.PCS1	1		SOC.L21
J2.80		spi3.SCK	1		SOC.N18
J2.87		spi3.SIN	1		SOC.M21
J2.48		spi3.SOUT	1		SOC.N17

8.10.4 LPSPI4 Signals

Table 37: LPSPI4 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
J2.40		spi4.PCS0	5		SOC.R18
J2.46		spi4.PCS1	5		SOC.R20
J2.38		spi4.PCS2	5		SOC.R21
J2.44		spi4.SCK	5		SOC.T21
J2.34		spi4.SIN	5		SOC.R17
J2.36		spi4.SOUT	5		SOC.T20

8.10.5 LPSPI5 Signals

Table 38: LPSPI5 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
J2.40		spi5.PCS0	4		SOC.R18
J2.54		spi5.PCS1	6		SOC.W21
J2.44		spi5.SCK	4		SOC.T21
J2.34		spi5.SIN	4		SOC.R17
J2.36		spi5.SOUT	4		SOC.T20

8.10.6 LPSPI6 Signals

Table 39: LPSPI6 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
J3.30		spi6.PCS0	4		SOC.J21
J3.64		spi6.PCS1	6		SOC.U21
J3.58		spi6.SCK	4		SOC.K21
J3.50		spi6.SIN	4		SOC.J20
J3.38		spi6.SOUT	4		SOC.K20

8.10.7 LPSPI7 Signals

Table 40: LPSPI7 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
J2.86		spi7.PCS0	4		SOC.L17
J2.60		spi7.PCS1	6		SOC.V21
J1.17		spi7.SCK	4		SOC.L21
J2.85		spi7.SIN	4		SOC.L18
J1.19		spi7.SOUT	4		SOC.L20

8.10.8 LPSPI8 Signals

Table 41: LPSPI8 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
J2.79		spi8.PCS0	4		SOC.N20
J2.42		spi8.PCS1	6		SOC.V20
J2.77		spi8.SCK	4		SOC.P21
J2.81		spi8.SIN	4		SOC.N21
J2.83		spi8.SOUT	4		SOC.P20

8.11 FlexSPI - Flexible Serial Peripheral Interface

The DART-MX91 exposes one FlexSPI module which can be used to interface external serial flash devices.

The module contains the following features:

- Flexible sequence engine to support various flash vendor devices
- Single pad/Dual pad/Quad pad mode of operation
- Single Data Rate/Double Data Rate mode of operation
- DMA support
- Memory mapped read access to connected flash devices

Note: *To use FLexSPI a special assembly module should be ordered.*
The module should not have a Wi-Fi option assembled,
and SDEX assembly option should be selected.
FlexSPI signals are referenced to 1.8v.

8.11.1 FlexSPI Signals

Table 42: FlexSPI Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
J2.35	SDEX	flexspi.A_DATA[0]	1	Runs @ 1.8V.	SOC.T16
J2.33	SDEX	flexspi.A_DATA[1]	1	Runs @ 1.8V.	SOC.V14
J2.31	SDEX	flexspi.A_DATA[2]	1	Runs @ 1.8V.	SOC.U14
J2.29	SDEX	flexspi.A_DATA[3]	1	Runs @ 1.8V.	SOC.T14
J2.45	SDEX	flexspi.A_SCLK	1	Runs @ 1.8V.	SOC.V16
J2.43	SDEX	flexspi.A_SS0_B	1	Runs @ 1.8V.	SOC.U16

8.12 TPM - Timer/PWM Module

The DART-MX91 exports up to 6 TPM channels.
The TPM (Timer/PWM Module) is a 4-channel timer that supports input capture, output compare, and the generation of PWM signals to control electric motor and power management applications. The counter, compare and capture registers are clocked by an asynchronous clock that can remain enabled in low power modes.

PWM Features:

- TPM clock mode is selectable
  - Can increment on every edge of the asynchronous counter clock
  - Can increment on rising edge of an external clock input synchronized to the asynchronous counter clock
- Pre-scaler divide-by 1, 2, 4, 8, 16, 32, 64, or 128
- TPM includes a 32-bit TPM counter
  - It can be a free-running counter or modulo counter
  - The counting can be up or up-down
- Includes 4 channels that can be configured as follows:
  - Input capture mode: the capture can occur on rising edges, falling edges or both edges
  - Output compare mode: the output signal can be set, cleared, pulsed, or toggled on match
- Edge-aligned or center-aligned PWM mode for all channels
- Support the generation of an interrupt and/or DMA request per channel
- Support the generation of an interrupt and/or DMA request when the counter overflows
- Support selectable trigger input to optionally reset or cause the counter to start incrementing.
  - The counter can also optionally stop incrementing on counter overflow
- Support the generation of hardware triggers when the counter overflows and per channel

8.12.1 TPM1 Signals

Table 43: TPM1 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
J2.88		tpm1.CH0	3	Used as console debug on Variscite release.	SOC.E20
J2.90		tpm1.CH1	3	Used as console debug on Variscite release. BOOT_MODE0 pin. Do not drive until after POR_B rise + 30ms. Internal buffer connected to J2.78 drives this pin, latched with POR_B rise.	SOC.E21
J2.16	Non-AC	tpm1.CH2	3		SOC.F20
J2.56		tpm1.EXTCLK	3		SOC.J17

8.12.2 TPM2 Signals

Table 44: TPM2 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
J2.32		tpm2.CH0	3		SOC.C20
J2.30		tpm2.CH1	3		SOC.C21
J2.6	Non-AC	tpm2.CH2	3		SOC.D20
J2.8	Non-AC	tpm2.CH3	3		SOC.D21
J3.62		tpm2.EXTCLK	3		SOC.G18

8.12.3 TPM3 Signals

Table 45: TPM3 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
J2.86		tpm3.CH0	1		SOC.L17
J2.36		tpm3.CH1	6		SOC.T20
J2.79		tpm3.CH2	1		SOC.N20
J3.64		tpm3.CH3	4		SOC.U21
J2.87		tpm3.EXTCLK	4		SOC.M21

8.12.4 TPM4 Signals

Table 46: TPM4 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
J2.85		tpm4.CH0	1		SOC.L18
J2.44		tpm4.CH1	6		SOC.T21
J2.81		tpm4.CH2	1		SOC.N21
J2.60		tpm4.CH3	4		SOC.V21
J2.48		tpm4.EXTCLK	4		SOC.N17

8.12.5 TPM5 Signals

Table 47: TPM5 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
J1.19		tpm5.CH0	1		SOC.L20
J3.42		tpm5.CH1	4		SOC.U18
J2.40		tpm5.CH2	6		SOC.R18
J2.42		tpm5.CH3	4		SOC.V20
J2.80		tpm5.EXTCLK	4		SOC.N18

8.12.6 TPM6 Signals

Table 48: TPM6 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
J2.89		tpm6.CH0	4		SOC.M20
J3.46		tpm6.CH1	4		SOC.U20
J2.34		tpm6.CH2	6		SOC.R17
J2.54		tpm6.CH3	4		SOC.W21
J3.42		tpm6.EXTCLK	5		SOC.U18

8.13 LPI2C - Low Power Inter-Integrated Circuit

The DART-MX91 exposes up to seven I2C Interfaces provides access to external serial devices.

The I2C (Inter-Integrated Circuit) serial bus is multi-controller, multi-target, packet-switched, and single-ended, and is often used to attach microcontroller ICs to lower-speed peripheral ICs.

LPI2C is a low-power Inter-Integrated Circuit (I2C) module that supports an efficient interface to an I2C bus as a controller and/or as a target. The LPI2C module also complies with the System Management Bus (SMBus) Specification, version 3. The SMBus is a single-ended simple two-wire bus, which is typically used for low-bandwidth communications.

The LPI2C has the following key features:

- Standard, Fast, Fast+ and Ultra-Fast modes
- High-speed mode (HS) in target mode
- Multi-controller, including synchronization and arbitration. Multi-controller means that any number of controller nodes can be present. Additionally, controller and target roles may be changed between messages (after a STOP is sent).
- Clock stretching. Sometimes multiple I2C nodes may drive the lines at the same time. If any I2C node is driving a line low, then that line is low. I2C nodes that are starting to transmit a logical one (by letting the line float high) can detect that the line is low. In this way, the nodes can identify that another I2C node is active at the same time.
    - When node detection is used on the SCL line, it is called clock stretching. Clock stretching is used as an I2C flow control mechanism.
    - When node detection is used on the SDA line, it is called arbitration. Arbitration ensures that there is only one I2C node transmitter at a time.
- General call, seven-bit addressing, and ten-bit addressing
- Software reset, START byte, and Device ID (also require software support)

8.13.1 LPI2C1 Signals

Table 49: LPI2C1 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
J1.13		i2c1.SCL	6	Runs @ 3. 3V. Routed through PMIC internal voltage translator. Has an internal 1.47K pull up	SOC.AA11
J2.32		i2c1.SCL	0		SOC.C20
J1.74		i2c1.SCL	3	External SD card detect input. Will change level according to J1.90 NVCC_SD	SOC.Y17
J1.11		i2c1.SDA	6	Runs @ 3. 3V. Routed through PMIC internal voltage translator. Has an internal 1.47K pull up	SOC.AA10
J2.30		i2c1.SDA	0		SOC.C21
J1.82		i2c1.SDA	3	Will change level according to J1.90 NVCC_SD	SOC.AA19

8.13.2 LPI2C2 Signals

Table 50: LPI2C2 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
J1.8	Non-EC	i2c2.SCL	6	Runs @ 1.8V	SOC.V12
J2.6	Non-AC	i2c2.SCL	0		SOC.D20
J1.6	Non-EC	i2c2.SDA	6	Runs @ 1.8V	SOC.U12
J2.8	Non-AC	i2c2.SDA	0		SOC.D21

8.13.3 LPI2C4 Signals

Table 51: LPI2C4 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
J2.29	SDEX	i2c4.SCL	2	Runs @ 1.8V	SOC.T14
J3.58		i2c4.SCL	1		SOC.K21
J2.31	SDEX	i2c4.SDA	2	Runs @ 1.8V	SOC.U14
J3.38		i2c4.SDA	1		SOC.K20

8.13.4 LPI2C5 Signals

Table 52: LPI2C5 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
J3.50		i2c5.SCL	6		SOC.J20
J3.46		i2c5.SCL	6		SOC.U20
J3.42		i2c5.SDA	6		SOC.U18
J3.30		i2c5.SDA	6		SOC.J21

8.13.5 LPI2C6 Signals

Table 53: LPI2C6 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
J2.85		i2c6.SCL	6		SOC.L18
J3.58		i2c6.SCL	6		SOC.K21
J2.86		i2c6.SDA	6		SOC.L17
J3.38		i2c6.SDA	6		SOC.K20

8.13.6 LPI2C7 Signals

Table 54: LPI2C7 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
J2.87		i2c7.SCL	6		SOC.M21
J1.17		i2c7.SCL	6		SOC.L21
J2.89		i2c7.SDA	6		SOC.M20
J1.19		i2c7.SDA	6		SOC.L20

8.13.7 LPI2C8 Signals

Table 55: LPI2C8 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
J2.80		i2c8.SCL	6		SOC.N18
J2.81		i2c8.SCL	6		SOC.N21
J2.48		i2c8.SDA	6		SOC.N17
J2.79		i2c8.SDA	6		SOC.N20

8.14 I3C - Improved Inter-Integrated Circuit

The MIPI Alliance Improved Inter-Integrated Circuit (MIPI I3C) improves upon the use and power of I2C, and provides an alternative to SPI for mid-speed applications.
The I3C bus protocol supports:

- In-band interrupts (IBI). These interrupts go from target to controller without extra wires, and the controller knows which target sent the interrupt.
- Common Command Codes (CCC)
- Dynamic addressing
- Multi-controller/multi-drop
- Hot-Join (HJ)
- I2C compatibility

The I3C peripheral supports all required and most optional features of the MIPI Alliance Specification for I3C, v1.0 and v1.1, except for ternary data rates (HDR-TSP and HDR-TSL).

The I3C module has the following key features:

- Two-wire multi-drop bus capable of 12.5 MHz clock speeds, with up to 11 devices.
    - Uses standard pads with 4 mA drive.
    - Dynamically assigns target addresses, and targets do not require static addresses. However, targets may have an I2C static address assigned at start-up, so the target can operate on an I2C bus. By default, I3C supports seven-bit I2C-style addresses.
    - Supports extended I2C 10-bit addressing through Map Feature Control 1 (SMAPCTRL1) register.
    - Allows targets to use the inbound SCL clock as the peripheral clock (instead of the clock from the controller) so devices can have slow or inaccurate clocks internally.
    - Allows simple targets, such as temperature sensors, to have no internal clock.
    - I3C controller supports handoff from Open Drain to Push-Pull mode for ACK to data transfer.
    - Normally the controller terminates the read, but for I3C, the target can also end the read.
- In-Band Interrupts (IBI) allow targets to send notifications to a controller.
    - Can be equivalent to a separate GPIO, but can also be directly data-bearing.
    - Can be prioritized. When multiple targets send interrupts to a controller at the same time, the order is resolved. Dynamic addresses establish the priority of the targets, so the controller controls the priority of the targets. Targets with lower-value dynamic addresses are higher priority level IBIs.
    - Can start interrupts even when the controller is not active on the bus. No free-running clock is needed, but starting an interrupt requires a Bus Available condition.
    - Can resolve an initial event via a time-stamping option, not requiring an interrupt.
- Built-in commands are in a separate space. These commands do not collide with normal controller-to-target messages.
    - Controls bus behavior, modes and states, low-power state, inquiries, and more.
    - Has additional room for new built-in commands to be used by other groups.
- Organized forms of multi-controller modes:
    - Secondary controllers, which use clean handoffs between different controllers.
- Hot-join onto I3C bus allows devices to connect to the bus later than when the bus starts.

  - Enables a device or module to get onto the I3C bus when it woke up after power-up or was physically inserted onto the I3C bus.
  - Provides a clean method for notification when new devices or modules get onto the I3C bus.
- Can use both I2C and I3C buses.
  - I3C supports specific legacy I2C devices on the bus.
  - I3C target devices can operate on I2C buses.
  - Supports bridging to I2C, SPI, UART, and other buses.
- Higher data rate modes are available.
  - Has a High Data Rate - Double Data Rate (HDR-DDR) mode, which is double the data rate of SDR (about 20 Mbit/s)
  - Only the controller and the specific target must support the higher data rate. The other targets can ignore it.

The I3C peripheral supports the full I3C feature set, except for the ternary data rates (HDR-TSP and HDR-TSL).

8.14.1 I3C1 Signals

Table 56: I3C1 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
J2.6	Non-AC	i3c1.PUR	1		SOC.D20
J2.6	Non-AC	i3c1.PUR_B	6		SOC.D20
J2.32		i3c1.SCL	1		SOC.C20
J2.30		i3c1.SDA	1		SOC.C21

8.14.2 I3C2 Signals

Table 57: I3C2 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
J1.2	Non-EC	i3c2.PUR	2	Runs @ 1.8V.	SOC.T12
J1.88		i3c2.PUR	2	Will change level according to J1.90 NVCC_SD.	SOC.Y19
J1.2	Non-EC	i3c2.PUR_B	6	Runs @ 1.8V.	SOC.T12
J1.88		i3c2.PUR_B	3	Will change level according to J1.90 NVCC_SD.	SOC.Y19
J1.13		i3c2.SCL	2	Runs @ 3.3V. Routed through PMIC internal voltage translator. Has an internal 1.47K pull up.	SOC.AA11
J1.74		i3c2.SCL	2	External SD card detect input. Will change level according to J1.90 NVCC_SD.	SOC.Y17
J1.11		i3c2.SDA	2	Runs @ 3.3V. Routed through PMIC internal voltage translator. Has an internal 1.47K pull up.	SOC.AA10
J1.82		i3c2.SDA	2	Will change level according to J1.90 NVCC_SD.	SOC.AA19

8.15 GPIO - General-Purpose Input/Output

The DART-MX91 exposes up to 85 General-Purpose Input/Output pins.

The GPIO module has the following key features:

- Port Data Input (PDIR) register displays the logic value on each pin when the pin is configured for any digital function provided the corresponding Port Control and Interrupt module for that pin are enabled.
- Port Data Output (PDOR) register with corresponding set/clear/toggle registers controls output data of each pin when the pin is configured for the GPIO function.
- Port Data Direction (PDDR) register controls the direction of each pin when the pin is configured for the GPIO function.
- Port Input Disable (PIDR) register controls the disable of the input for each general-purpose pin.
- Pin interrupts
    - Interrupt flag and enable registers for each pin are functional in all digital pin muxing modes.
    - Support for interrupt or DMA request configured per pin.
    - Support for edge sensitive (rising or falling, or both) or level sensitive (low, high) configured per pin.
    - Asynchronous wake-up in Low-Power modes.
    - GPIO module generates a total of 2 interrupts and 2 DMA requests.
    - Each pin can be used to generate a single interrupt or DMA request.
- Protection registers
    - Each pin is configured for Secure or Non-Secure and Privilege/Non-Privilege access.
    - Each interrupt and DMA request domain is configured for Secure or Non-Secure and Privilege/Non-Privilege access.

8.15.1.1 GPIO Signals

Table 58: GPIO Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
J2.32		gpio1.IO[0]	5		SOC.C20
J2.30		gpio1.IO[1]	5		SOC.C21
J3.62		gpio1.IO[10]	5		SOC.G18
J2.10		gpio1.IO[11]	5	BOOT_MODE2 pin. Has an internal SOC PD. Do not drive until after POR_B rise + 30ms	SOC.G21
J2.4	Non-AC	gpio1.IO[12]	5		SOC.G20
J2.14	Non-AC	gpio1.IO[13]	5	BOOT_MODE3 pin. Has an internal SOC PD. Do not drive until after POR_B rise + 30ms.	SOC.H21
J2.2	Non-AC	gpio1.IO[14]	5		SOC.H20
J2.28		gpio1.IO[15]	5		SOC.J18
J2.6	Non-AC	gpio1.IO[2]	5		SOC.D20
J2.8	Non-AC	gpio1.IO[3]	5		SOC.D21
J2.88		gpio1.IO[4]	5	Used as console debug on Variscite release.	SOC.E20
J2.90		gpio1.IO[5]	5	Used as console debug on Variscite release. BOOT_MODE0 pin. Do not drive until after POR_B rise + 30ms. Internal buffer connected to J2.78 drives this pin, latched with POR_B rise.	SOC.E21
J2.16	Non-AC	gpio1.IO[6]	5		SOC.F20
J2.50		gpio1.IO[8]	5		SOC.G17
J2.56		gpio1.IO[9]	5		SOC.J17
J3.30		gpio2.IO[0]	0		SOC.J21
J2.48		gpio2.IO[10]	0		SOC.N17
J3.50		gpio2.IO[1]	0		SOC.J20
J2.80		gpio2.IO[11]	0		SOC.N18
J2.79		gpio2.IO[12]	0		SOC.N20
J2.81		gpio2.IO[13]	0		SOC.N21
J2.83		gpio2.IO[14]	0		SOC.P20
J2.77		gpio2.IO[15]	0		SOC.P21
J2.38		gpio2.IO[16]	0		SOC.R21
J2.46		gpio2.IO[17]	0		SOC.R20
J2.40		gpio2.IO[18]	0		SOC.R18
J2.34		gpio2.IO[19]	0		SOC.R17
J2.36		gpio2.IO[20]	0		SOC.T20
J3.38		gpio2.IO[2]	0		SOC.K20
J2.44		gpio2.IO[21]	0		SOC.T21
J3.42		gpio2.IO[22]	0		SOC.U18
J3.46		gpio2.IO[23]	0		SOC.U20

Pin#	Assy	Pin Function	Alt#	Notes	Ball
J3.64		gpio2.IO[24]	0		SOC.U21
J2.60		gpio2.IO[25]	0		SOC.V21
J2.42		gpio2.IO[26]	0		SOC.V20
J2.54		gpio2.IO[27]	0		SOC.W21
J3.58		gpio2.IO[3]	0		SOC.K21
J2.86		gpio2.IO[4]	0		SOC.L17
J2.85		gpio2.IO[5]	0		SOC.L18
J1.19		gpio2.IO[6]	0		SOC.L20
J1.17		gpio2.IO[7]	0		SOC.L21
J2.89		gpio2.IO[8]	0		SOC.M20
J2.87		gpio2.IO[9]	0		SOC.M21
J1.74		gpio3.IO[0]	5	Will change level according to J1.90 NVCC_SD.	SOC.Y17
J1.82		gpio3.IO[1]	5	Will change level according to J1.90 NVCC_SD.	SOC.AA19
J1.88		gpio3.IO[2]	5	Will change level according to J1.90 NVCC_SD.	SOC.Y19
J2.45	SDEX	gpio3.IO[20]	5	Runs @ 1.8V.	SOC.V16
J2.43	SDEX	gpio3.IO[21]	5	Runs @ 1.8V.	SOC.U16
J2.35	SDEX	gpio3.IO[22]	5	Runs @ 1.8V.	SOC.T16
J2.33	SDEX	gpio3.IO[23]	5	Runs @ 1.8V.	SOC.V14
J2.31	SDEX	gpio3.IO[24]	5	Runs @ 1.8V.	SOC.U14
J2.29	SDEX	gpio3.IO[25]	5	Runs @ 1.8V.	SOC.T14
J2.76		gpio3.IO[26]	5	Runs @ 1.8V. Has an internal 12K pull down.	SOC.AA2
J3.48		gpio3.IO[27]	5	Runs @ 1.8V.	SOC.Y3
J2.24		gpio3.IO[28]	5	Runs @ 1.8V. Used on DART for BT communication. If BT not required internal buffer can be disabled, and pin function released to customer usage.	SOC.W1
J2.22		gpio3.IO[29]	5	Runs @ 1.8V. Used on DART for BT communication. If BT not required internal buffer can be disabled, and pin function released to customer usage.	SOC.W2
J1.86		gpio3.IO[3]	5	Will change level according to J1.90 NVCC_SD.	SOC.Y18
J2.26		gpio3.IO[3]	5	Runs @ 1.8V. Used on DART for BT communication. If BT not required internal buffer can be disabled, and pin function released to customer usage.	SOC.Y1
J2.20		gpio3.IO[31]	5	Runs @ 1.8V. Used on DART for BT communication. If BT not required internal buffer can be disabled, and pin function released to customer usage.	SOC.Y2
J1.80		gpio3.IO[4]	5	Will change level according to J1.90 NVCC_SD.	SOC.AA18
J1.78		gpio3.IO[5]	5	Will change level according to J1.90 NVCC_SD.	SOC.Y20
J1.84		gpio3.IO[6]	5	Will change level according to J1.90 NVCC_SD.	SOC.AA20
J2.25	SDEX	gpio3.IO[7]	5	Runs @ J1.90 VDD_SDIO2 level.	SOC.AA17
J1.13		gpio4.IO[0]	5	Runs @ 3.3V. Routed through PMIC internal voltage translator. Has an internal 1.47K pull up.	SOC.AA11

Pin#	Assy	Pin Function	Alt#	Notes	Ball
J1.10	Non-EC	gpio4.IO[10]	5	Runs @ 1.8V.	SOC.AA8
J1.11		gpio4.IO[1]	5	Runs @ 3.3V. Routed through PMIC internal voltage translator. Has an internal 1.47K pull up.	SOC.AA10
J1.12	Non-EC	gpio4.IO[11]	5	Runs @ 1.8V.	SOC.Y9
J1.14	Non-EC	gpio4.IO[12]	5	Runs @ 1.8V.	SOC.AA9
J1.16	Non-EC	gpio4.IO[13]	5	Runs @ 1.8V.	SOC.Y10
J2.27	SDEX	gpio4.IO[15]	5	Runs @ 1.8V.	SOC.AA6
J2.73		gpio4.IO[16]	5	Runs @ 1.8V.	SOC.T10
J2.78		gpio4.IO[17]	5	Runs @ 1.8V. Internal buffer connected to this pin drives BOOT_MODE0 (J2.90), latched with POR_B rise.	SOC.V8
J2.67		gpio4.IO[18]	5	Runs @ 1.8V.	SOC.U8
J2.70		gpio4.IO[19]	5	Runs @ 1.8V.	SOC.T8
J1.8	Non-EC	gpio4.IO[2]	5	Runs @ 1.8V.	SOC.V12
J2.74		gpio4.IO[20]	5	Runs @ 1.8V.	SOC.V6
J2.71		gpio4.IO[21]	5	Runs @ 1.8V.	SOC.U6
J2.64		gpio4.IO[22]	5	Runs @ 1.8V.	SOC.Y4
J2.72		gpio4.IO[23]	5	Runs @ 1.8V.	SOC.AA3
J2.65		gpio4.IO[24]	5	Runs @ 1.8V.	SOC.AA4
J2.69		gpio4.IO[25]	5	Runs @ 1.8V.	SOC.Y5
J2.66		gpio4.IO[26]	5	Runs @ 1.8V.	SOC.AA5
J2.68		gpio4.IO[27]	5	Runs @ 1.8V.	SOC.Y6
J1.28		gpio4.IO[28]	5	Runs @ 1.8V.	SOC.U4
J3.52		gpio4.IO[29]	5	Runs @ 1.8V.	SOC.V4
J1.6	Non-EC	gpio4.IO[3]	5	Runs @ 1.8V.	SOC.U12
J1.2	Non-EC	gpio4.IO[4]	5	Runs @ 1.8V.	SOC.T12
J1.4	Non-EC	gpio4.IO[5]	5	Runs @ 1.8V.	SOC.W11
J1.3	Non-EC	gpio4.IO[6]	5	Runs @ 1.8V.	SOC.V10
J1.5	Non-EC	gpio4.IO[7]	5	Runs @ 1.8V.	SOC.U10
J1.9	Non-EC	gpio4.IO[8]	5	Runs @ 1.8V.	SOC.Y8
J1.7	Non-EC	gpio4.IO[9]	5	Runs @ 1.8V. Has EMI filter.	SOC.AA7

8.16 LPTMR - Low-Power Timer

The low-power timer (LPTMR) can be configured to operate as a time counter with optional prescaler, or as a pulse counter with optional glitch filter, across all power modes, including the low-power modes. It is reset only on Power on Reset (POR) or Low Voltage Detect (LVD), allowing it to be used as a time-of-day counter.

The LPTMR module has the following key features:

- 32-bit time counter or pulse counter with compare

  - Optional interrupt can generate asynchronous wake-up from any low-power mode.
  - Hardware trigger output.
  - Counter supports free-running mode or reset on compare.
- Configurable clock source for prescaler/glitch filter
- Configurable input source for pulse counter
  - Rising-edge or falling-edge

8.16.1 LPTMR1 Signals

Table 59: LPTMR1 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
J2.50		lptmr1.ALT1	4		SOC.G17
J2.56		lptmr1.ALT2	4		SOC.J17
J3.62		lptmr1.ALT3	4		SOC.G18

8.16.2 LPTMR2 Signals

Table 60: LPTMR2 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
J1.12	Non-EC	lptmr2.ALT1	3	Runs @ 1.8V.	SOC.Y9
J1.84		lptmr2.ALT1	1	Will change level according to J1.90 NVCC_SD.	SOC.AA20
J1.14	Non-EC	lptmr2.ALT2	3	Runs @ 1.8V.	SOC.AA9
J2.25	SDEX	lptmr2.ALT2	1	Runs @ J1.90 VDD_SDIO2 level.	SOC.AA17
J1.16	Non-EC	lptmr2.ALT3	3	Runs @ 1.8V.	SOC.Y10

8.17 Reference Clocks

The DART-MX91 exposes the clock outputs from the internal CCM module which can be used to clock external devices.

8.17.1 Clock Signals

Table 61: Clock Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
J2.76		ccmsrcgpcmix.CLKO1	0	Runs @ 1.8V. Has an internal 12K pull down.	SOC.AA2
J3.48		ccmsrcgpcmix.CLKO2	0	Runs @ 1.8V.	SOC.Y3
J1.28		ccmsrcgpcmix.CLKO3	0	Runs @ 1.8V.	SOC.U4
J3.52		ccmsrcgpcmix.CLKO4	0	Runs @ 1.8V.	SOC.V4

8.18 ADC

The DART-MX91 integrates 1 ADC. The main features are:

- It includes eight channels, four of them connected to pins in the package.
- Support the 1MS/s frequency of operation
- Multiple modes of starting conversion (Normal, Injected)
- Normal mode supports One-Shot and Scan (continuous) conversions
- Injected mode supports One-Shot conversions only
- Support TRGMUX to allow 16 trigger channels to be used by any ADC channel

8.18.1 ADC Signals

Table 62: ADC Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
J3.76		anamix.adc_in0	0	Runs @ 1.8V.	SOC.B19
J3.78		anamix.adc_in1	0	Runs @ 1.8V.	SOC.A20
J3.80		anamix.adc_in2	0	Runs @ 1.8V.	SOC.B20
J3.82		anamix.adc_in3	0	Runs @ 1.8V.	SOC.B21

8.19 DAP - Debug Access Port

DAP is a standard Arm component, comprising of several components. These components are used to access the DAP from an external debugger and Access Ports to access on-chip debug system resources. The DAP supports 1149.1/Arm SW-DP interface, which means that the JTAG interface can be operate in standard 5-pin JTAG-DP interface or in 2-pin SW-DP interface. The following figure shows the connectivity between the DAP and the pads.

8.19.1 DAP Signals

Table 63: DAP Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
J2.26		dap.TCLK_SWCLK	0	Runs @ 1.8V. Used on DART for BT communication. If BT not required internal buffer can be disabled, and pin function released to customer usage	SOC.Y1
J2.60		dap.TCLK_SWCLK	5		SOC.V21
J2.24		dap.TDI	0	Runs @ 1.8V. Used on DART for BT communication. If BT not required internal buffer can be disabled, and pin function released to customer usage	SOC.W1
J2.42		dap.TDI	5		SOC.V20
J2.20		dap.TDO_TRACESWO	0	Runs @ 1.8V. Used on DART for BT communication. If BT not required internal buffer can be disabled, and pin function released to customer usage	SOC.Y2
J3.64		dap.TDO_TRACESWO	5		SOC.U21
J2.22		dap.TMS_SWDIO	0	Runs @ 1.8V. Used on DART for BT communication. If BT not required internal buffer can be disabled, and pin function released to customer usage. Has an internal 10K pull down.	SOC.W2
J2.54		dap.TMS_SWDIO	5		SOC.W21

8.20 Power

8.20.1 Power

Table 64: Power

Pin#	Assy	Pin Function	Alt#	Notes	Ball
J3.71		VBAT			
J3.73		VBAT			
J3.75		VBAT			
J3.77		VBAT			
J3.79		VBAT			
J3.81		VBAT			
J3.83		VBAT			
J3.85		VBAT			
J3.87		VBAT			
J3.89		VBAT			
J1.15		NVCC_BBSM			PCA9451.3
J1.90		NVCC_SD		Power output for SD2 pins reference. 1.8V/3.3V- set by DART PMIC.	PCA9451.55
J3.66		USB1_VBUS		Runs @ 5.0V. VBUS Reference Voltage input.	SOC.F12
J3.26		USB2_VBUS		Runs @ 5.0V. VBUS Reference Voltage input.	SOC.E14

8.20.2 Ground

Table 65: Digital Ground Pins

Pin#	Assy	Pin Function	Alt#	Notes	Ball
J2.12		AGND	0		
J1.18		GND	0		
J1.21		GND	0		
J1.30		GND	0		
J1.33		GND	0		
J1.49		GND	0		
J1.52	Non-BTRST	GND	0		
J1.55	Non-WBE	GND	0		
J1.58	Non-WRST	GND	0		
J1.61	Non-WBE	GND	0		
J1.64	Non WBD/WBE	GND	0		
J1.67	Non WBE	GND	0		
J1.70	Non-BTRST	GND	0		
J1.76		GND	0		
J1.85		GND	0		
J2.18		GND	0		
J2.23		GND	0		
J2.47		GND	0		
J2.53		GND	0		
J2.75		GND	0		
J2.84		GND	0		
J3.9		GND	0		
J3.10		GND	0		
J3.15		GND	0		
J3.21		GND	0		
J3.24		GND	0		
J3.27		GND	0		
J3.33		GND	0		
J3.34		GND	0		
J3.39		GND	0		
J3.45		GND	0		
J3.51		GND	0		
J3.57		GND	0		
J3.63		GND	0		
J3.68		GND	0		
J3.74		GND	0		

8.21 General System Control

8.21.1 General System Control Signals

Table 66: General System Control Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
J1.1		PMIC_NINT	0	Runs @ 1.8V. Has an internal 100K pull up.	PCA9451.13
J3.88		PMIC_ON_REQ	0	Runs @ 1.8V.	SOC.A17
J1.22		PMIC_RST_B	0	Runs @ 1.8V. PMIC reset input. Pull low to hold DART internal regulators OFF. Pulse low for **cold** reboot. Has an internal 100K pull up.	PCA9451.8
J1.26		PMIC_STBY_REQ	0	Runs @ 1.8V.	SOC.B18
J1.20		ONOFF	0	Runs @ 1.8V.	SOC.A19
J1.24		POR_B	0	Runs @ 1.8V. Pull low to hold SOC in reset state. Pulse low for **warm** reboot. Has an internal 100K pull up.	PCA9451.9
J3.70		TAMPER0	0	Runs @ 1.8V.	SOC.B16
J3.72		TAMPER1	0	Runs @ 1.8V.	SOC.F14
J2.28		wdog1.WDOG_ANY	0		SOC.J18
J3.84		CLKIN1	0	Runs @ 1.8V. Has an internal 100K pull down.	SOC.B17
J3.86		CLKIN2	0	Runs @ 1.8V. Has an internal 100K pull down.	SOC.A18

8.21.2 Boot configuration

The DART-MX91 can be boot from the following sources:

- Internal source - eMMC Flash memory (J2.90 set to Low)
- External source
  - SD Card (J2.90 set to High and SD Card plugged in)
  - USB UUU Serial Downloader (J2.90 set to High and SD Card is not plugged in)

To select other boot modes the following pins can be used.
The BOOT_MODE[1] is not exposed and always pulled up on the SOM.

Table 67: BOOT_MODE Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
J2.10		BOOT_MODE[2]		Has an internal SOC PD. Do not drive until after POR_B rise + 30ms	SOC.G21
J2.14	Non-AC	BOOT_MODE[3]		Has an internal SOC PD. Do not drive until after POR_B rise + 30ms.	SOC.H21
J2.90		BOOT_MODE[0]		Used as console debug on Variscite release. Do not drive until after POR_B rise + 30ms Internal buffer connected to J2.78 drives this pin, latched with POR_B rise.	SOC.E21
J2.78		enet2.RGMII_TD2		Runs @ 1.8V. Internal buffer connected to this pin drives BOOT_MODE0 (J2.90). Latched with POR_B rise.	SOC.V8

Table 68: Available boot modes

BOOT_MODE [3:0]	BOOT CORE	BOOT DEVICE	Notes
0000	Cortex-A55	From internal fuses	
0001	Cortex-A55	USB1/2 Serial Downloader	**Can be achieved by J2.90 set to High and SD Card is not plugged in**
0010	Cortex-A55	USDHC1 8-bit eMMC 5.1	**Variscite EVK and SW support this mode**
0011	Cortex-A55	USDHC2 4-bit SD3.0	**Variscite EVK and SW support this mode**
0100	Cortex-A55	FlexSPI Serial NOR. Supports SFDP (JESD-216) parameters	
0101	Cortex-A55	FlexSPI Serial NAND 2K page	
0110	Cortex-A55	Infinite Loop	
0111	Cortex-A55	Test Mode	

9. Assembly Options

To make the solution as Flexible as possible the following assembly options were added. The assembly options help customers to order the SOM variant that includes only the needed interfaces with a lower cost.

9.1 Ethernet PHY

The SOM can be ordered without Ethernet PHY chip assembled; it allows reducing the overall cost of the product in case the Ethernet Interfaces are not used.
when not assembled, SoC balls are exported to SOM connector instead of Ethernet interface pins.

9.2 Analog Audio Codec

The SOM can be ordered without Audio Codec chip assembled. This allows reducing the overall cost of the product in case the Analog Audio Codec is not used.
when not assembled, SoC balls are exported to SOM connector instead of Analog codec interface pins.

9.3 Single/Dual band Wi-Fi and BT/BLE combo

The SOM can be ordered without the Single or Dual band Wi-Fi and BT/BLE combo chip assembled, it allows reducing the overall cost of the product in case the Wi-Fi and BT/BLE is not used.

9.4 LPDDR4

The SOM can be ordered with different RAM size capacities, it allows reducing the overall cost of the product in case lower RAM size is sufficient.

9.5 eMMC

The SOM can be ordered with different eMMC size capacities, it allows reducing the overall cost of the product in case lower eMMC size is sufficient.

10. Electrical Specifications

10.1 Absolute Maximum Ratings

Table 69: Absolute Maximum Ratings

Pin #	Min	Max	Units	Comments
VBAT	-0.3	6.0	V	
USB_OTG1_VBUS, USB_OTG2_VBUS	-0.3	5.25	V	
Vin/Vout input/output voltage range (GPIO Type Pins)	-0.3	OVDD+0.3		OVDD is the I/O supply voltage
ESD damage immunity Human Body Model (HBM)	--	TBD		
ESD damage immunity Charge Device Model (CDM)	--	TBD		

10.2 Operating Conditions

Table 70: Operating Ranges

Pin #	Min	Typ	Max	Unit
VCC_SOM	3.5	3.7	5.5	V
USB_OTG1_VBUS/ USB_OTG2_VBUS	4.75	5	5.25	V

10.3 Peripheral Voltage Levels

Most of the peripheral interface lines used as inputs or outputs to the DART-MX91 use 3.3V LVCMOS levels, except the following interfaces: SD2, ENET_QOS, and ENET.

***USB*:** The interface follows a USB standard.

uSDHC2: (SDIO lines) interface IOs will change voltage between 3.3V and 1.8V depending on the SD card capabilities.
With other alternative functions, the user can determine whether the voltage of the uSDHC2 IOs bank will be 1.8V or 3.3V using gpio3.IO[19].

ENET_QOS: interface available in case SOM is ordered **without "EC"** configuration.
IO voltage is 1/8V.

ENET1: IO voltage is 1/8V.

10.4 Power Consumption

Table 71: DART-MX91 Power Consumption

Mode	Voltage	Current	Power	Conditions
Run	3.84V	378mA	1.45W	Linux up, Wi-Fi connected and Iperf is running 802.11ax 5GHz
Run	3.84V	330mA	1.26W	Linux up, Wi-Fi connected and Iperf is running 802.11n 2.4GHz
Run	3.84V	320mA	1.22W	Linux up. Ethernet0 running Iperf
Run	3.84V	145mA	0.55W	Linux up. Ethernet0, Ethernet1, Wi-Fi module up
Standby	3.84V	TBD	TBD	Memory retention mode
Off (RTC)	3.84V	1.82mA	6.9mW	All power rails are Off, only Internal SoC RTC is powered

Note: *The Wi-Fi module needs a power source that can provide a peak current of ~1000mA@1.8V during DPD calibration when the firmware is downloaded, even though its max continuous supply current during transmission/reception is less.*
Module calibration occurs:

- *When the Module is initially powered up.*
- *The module is reset.*
- *When the radio is initialized.*
- *Every two minutes after the radio is initialized.*

NOTE

Setup:
HW: *DART-MX91S_1400C_2048R_16G_AC_EC_WBD_ET_REV1.0A*
SW: mx91-yocto-scarthgap-6.6.52_2.2.0-v1.3

DISCLAIMER:
The power consumption measurements apply only to limited operation scenarios. Actual power consumption may vary depending on the interfacing peripherals and user application modes; users must conduct testing according to their specific operation scenarios.

An appropriate thermal solution should be applied depending on the specific use cases and end-product system design.

11. Environmental Specifications

Table 72: Environmental Specifications

Parameter	Min	Max
Commercial Operating Temperature Range	0°C	70°C
Extended Operating Temperature Range	-25°C	85°C
Industrial Operating Temperature Range	-40°C	85°C
Storage Temperature Range	-40°C	85°C
Relative humidity (operation)	10%	90%
Relative humidity (storage)	05%	95%
MTBF Prediction Method Model: Telcordia Technologies Special Report SR-332, Issue 4 50°C, GB	> 5000 Khrs *	

Note: *Industrial Temperature is only based on the operating temperature grade of the SoM components. Customer should consider specific thermal design for the final product based upon the specific environmental and operational conditions.*

*Preliminary information

12. Mechanical

12.1 Carrier Board Mounting

The SOM has four mounting holes, which are plated holes connected to GND, for mounting it to the carrier board.

Note: *The size and footprint of SOM 90-pin connectors Hirose P/N: DF40C-90DP-0.4V(51) are different from mating carrier board 90-pin connectors (see section 7.1).*
To ensure the correct positioning of the carrier board connectors and holes, please refer to VAR-DT8MCustomBoard DXF is available here (under the documentation tab):
http://www.variscite.com/products/single-board-computers/var-dt8mcustomboard

It is recommended NOT to place any components under the SOM.

12.2 Standoffs

Customers requiring a mechanical solution for mounting in harsh vibration environments can use the following standoff:

Manufacturer: **MAC8**

PN: **TH-1.6-1.5-M2**

Link: http://www.mac8japan.com/English%20Catalog/TH1.6%20Series-2.pdf

12.3 SOM Dimensions

The connectors' size, mounting holes, and relative locations can be found in the figures below.
All dimensions are given in millimeter and [mils] units.

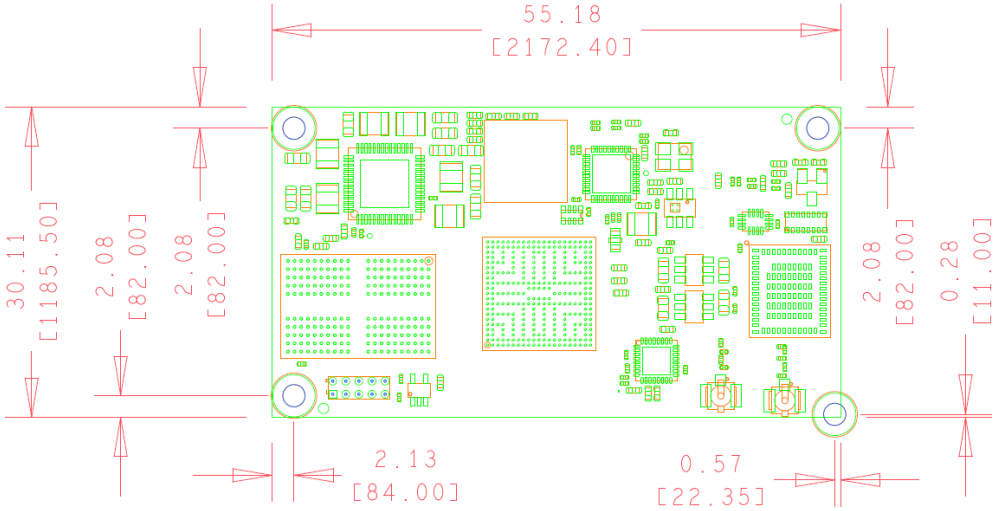


Figure 5: DART-MX91 Component Side Mechanics (Top view)

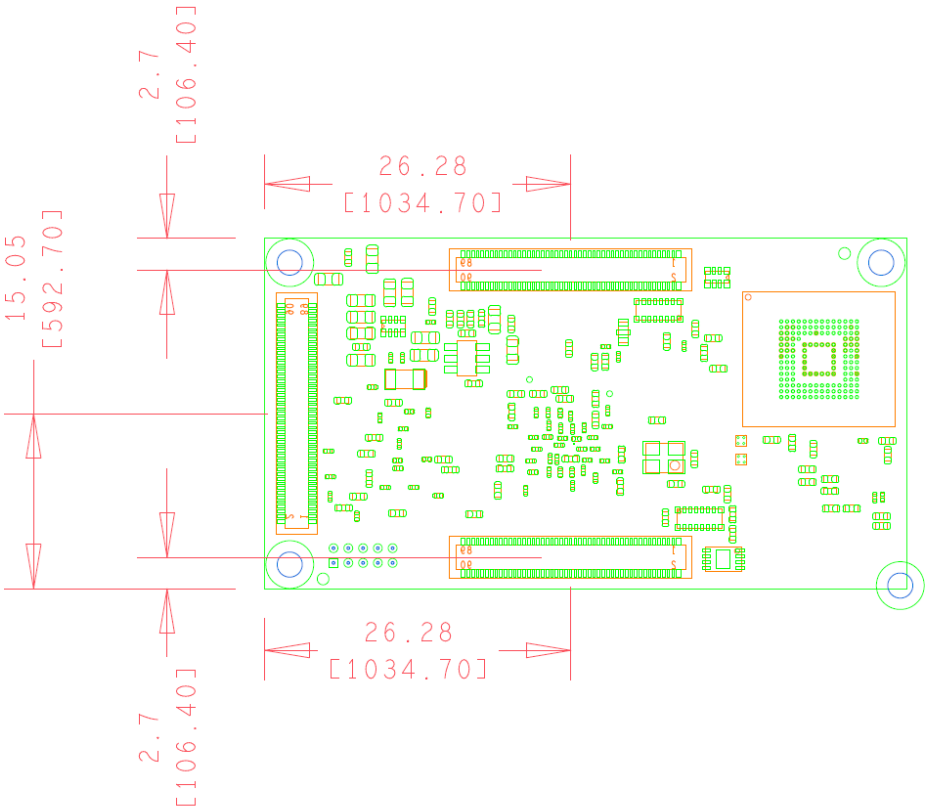


Figure 6: DART-MX91 Print Side Mechanics (Top view)

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