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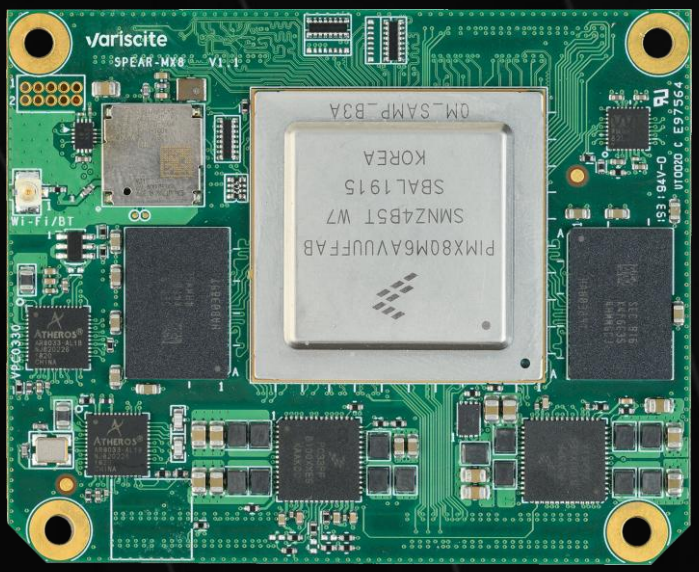
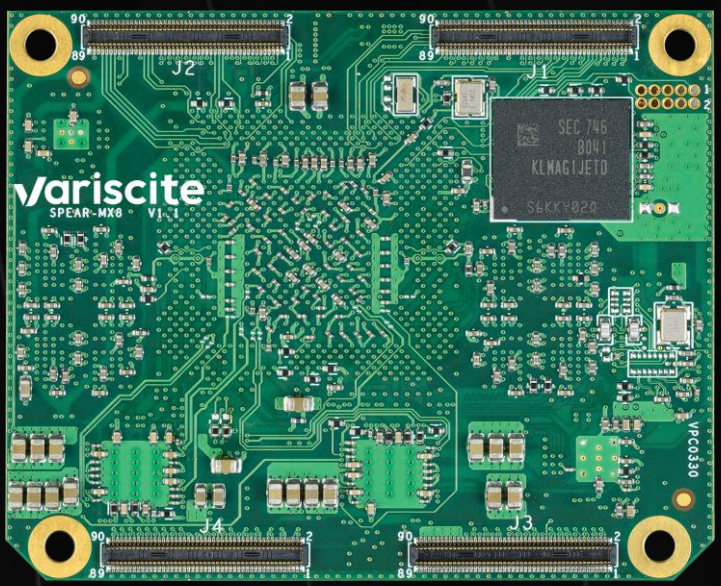
SPEAR-MX8 V1.x Datasheet

NXP i.MX 8QM™ - based System-on-Module





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SPEAR-MX8 Datasheet

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1 Document Revision History

Table 1: Revision History

Revision	Date	Notes
1.0	Jun 24, 2018	Initial - Preliminary
1.04	Oct 9, 2018	Pre-Release
1.05	Nov 29, 2018	CPU speed updated
1.1	Sep 19, 2019	Release: 1) J3 pinout change 2) Output power supplies section changed 3) DMIC lines voltage change
1.2	Feb 4, 2020	1) Block diagram changed to follow the design 2) J1.76, J1.78 Ball number changed 3) J1.76, J1.78, J4.47 GPIO number fixed
1.3	Jun 4, 2020	SPEAR-MX8 Power Consumption table changed
1.4	Sep 21, 2020	1) JTAG Pinout changed. Note added. 2) LDO3 Note added.
1.5	Nov 1, 2020	1) J3 pinout change to reflect correct RGMII bypass connections 2) RGMII Section updated to correct bypass connections 3) UART3 Table updated to reflect correct RGMII bypass connections
1.6	Jan 25, 2021	1) HDMI RX Section removed 2) MLB Section Removed Removed due to NXP PCN 202012002I
1.7	Jul 12, 2021	1) Updated section 9.7 Boot configuration table 2) Updated section 5.2.1
1.8	Sep 1, 2021	1) RGMII Section Voltage information added 2) EEPROM Information added
1.9	Nov 15, 2021	1) Updated section 4.3 Block diagram EERPROM, Ethernet PHY
1.10	Apr 26, 2022	1) Added Ethernet PHY ADIN1300 - Updated sections 4.3, 5.6, 7.3, 8.4 2) Updated section 5.3 1) Corrected Note [3] in Tables 6,7,54
1.11	May 1, 2022	Updated the sections: 4.2, 5.4
1.12	Jan 3, 2023	1) Updated Key Features section 5.4
1.13	Feb 26, 2023	1) Updated section 12 2) Updated the eMMC sections 4.2, 5.2
1.14	Aug 30, 2023	1) Updated section 4.2
1.15	Jan 29, 2024	1) Updated section 4.2 2)

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4 Overview

4.1 General Information

The SPEAR-MX8 offers high-performance processing for a low-power System-on-Module.
The product is based on the NXP i.MX8QM comprehensive multimedia device targeting high-end automotive and industrial market segments. The chip is built using a leading edge process to achieve both high performances and low-power consumption. The chip relies on a powerful fully-coherent core complex based on a dual (2x) Cortex-A72 cluster for use-cases requiring high computing performances and a quad (4x) Cortex-A53 cluster running most of the use cases at a lower-power consumption.
Graphics processing is handled by two (2x) Graphics Processing Units (GPU) supporting the latest graphic APIs including OpenVX for computer vision. Video is managed by a dedicated video engine decoding formats including HEVC (H.265) up to 4K60, and encoding in H.264 up to 1080p60. The chip provides various display interfaces that supports up to four displays.
This heterogeneous multicore processing architecture enables the device to run an open operating system like Linux and an RTOS like FreeRTOS™ on the Cortex-M4 core for time and security critical tasks.

The SPEAR-MX8 provides an ideal building block for simple integration with a wide range of products in target markets requiring high-performance processing with low power consumption, compact size and a very cost-effective solution.

Supporting products:

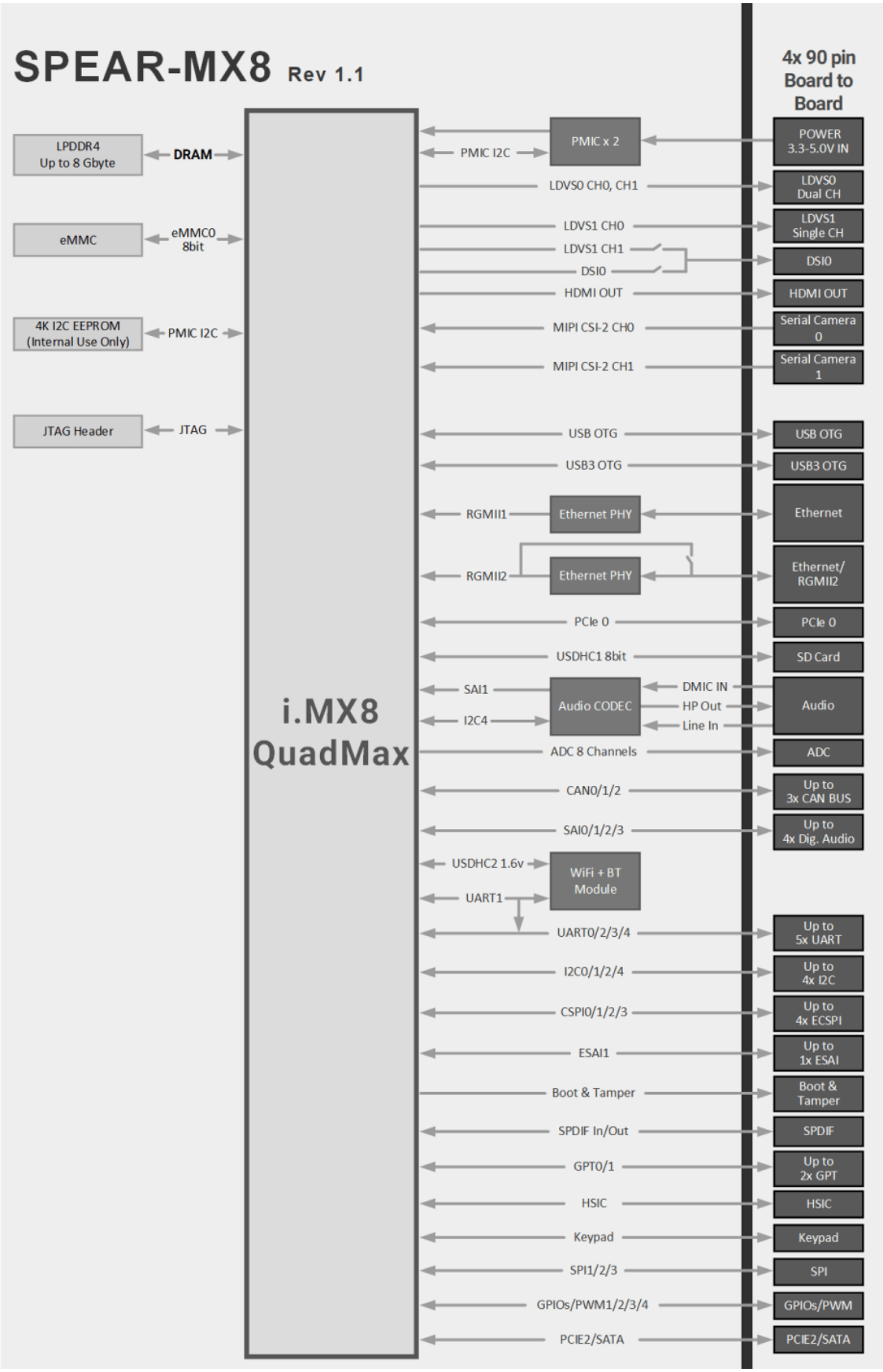
- SPEAR-MX8MCustomBoard – evaluation board
  - ✓ Carrier Board, compatible with SPEAR-MX8
  - ✓ Schematics
- VAR-DVK-SP8 full development kit, including:
  - ✓ SPEAR-MX8MCustomBoard
  - ✓ SPEAR-MX8
  - ✓ Display and touch
  - ✓ Accessories and cables
- O.S support
  - ✓ Linux BSP
  - ✓ Android

Contact Variscite support services for further information: mailto:support@variscite.com.

4.2 Feature Summary

- NXP i.MX8QM series SOC
  - 4x Cortex A53 up to @ 1.2 GHz at 1.0V
  - 2x Cortex A72 up to @ 1.6 GHz at 1.0V
  - 2x Cortex M4 @ 264 MHz
  - i.MX8QM 4 x Cortex A53, 2x Cortex A72
  - 264MHz ARM® Cortex™-M4
  - Up to 8GB LPDDR4 RAM @ 1600Mhz
  - 8-bit up to 128GB eMMC boot and storage
- Display Support
  - 1x LVDS TX 1080p capable
  - 1x LVDS TX 720p (optional 1080 if no DSI)
  - HDMI/eDP/DP
  - MIPI DSI with 4 data lanes
- Networking
  - 2x 10/100/1000 Mbit/s Ethernet Interface
  - Certified Wi-Fi 802.11 ac/a/b/g/n
  - Bluetooth: 5.2/BLE
- Camera
  - 2x CSI – CMOS Serial camera Interface 4 lanes each
- Audio
  - Analog Stereo line in
  - Analog headphones out
  - Digital microphone
  - 6x Digital audio (SAI, SPDIF)
- USB
  - 1x USB 3.0 OTG
  - 1x USB 2.0 OTG
  - 1x USB 2.0 HSIC
- Other Interfaces
  - SDIO/MMC
  - 2x PCIe v2.0
  - SATA
  - Serial interfaces (ECSPI, QSPI, I2C, UART, JTAG, CAN)
  - GPIOs
- Single power supply: 3.35V – 4.5V
- Dimensions (W x L x H): 55.0 mm x 68.0 mm x 4.7 mm
- Industrial temperature range -40ºC to 85ºC

4.3 Block Diagram



5 Main Hardware Components

This section summarizes the main hardware building blocks of the SPEAR-MX8.

5.1 NXP i.MX8QM

5.1.1 Overview

The i.MX8QM is a fully comprehensive multimedia device targeting high-end automotive and industrial market segments. The chip is built using a leading-edge process to achieve both high performances and low-power consumption. The chip relies on a powerful fully-coherent core complex based on a dual (2x) Cortex-A72 cluster for use-cases requiring high computing performances and a quad (4x) Cortex-A53 cluster running most of the use cases at a lower-power consumption.
Graphics processing is handled by two (2x) Graphics Processing Units (GPU) supporting the latest graphic APIs including OpenVX for computer vision. Video is managed by a dedicated video engine decoding formats including HEVC (H.265) up to 4K60 and encoding in H.264 up to 1080p60. The chip provides various display interfaces that supports up to four displays.
To feed data to those high demanding blocks, i.MX8QM has two DRAM controllers supporting DDR4 and LPDDR4 memory types.

The i.MX8QM provides additional computing resources and peripherals:

- A dedicated system control unit and a dedicated security subsystem which provides High Assurance Boot (HAB) features and cryptographic acceleration
- An audio sub-system with a wide range of audio interfaces
- Two general purpose Cortex-M4 with their own off-platform peripherals
- A large set of peripherals that are commonly used in automotive and industrial markets

5.1.2 i.MX8M Block Diagram

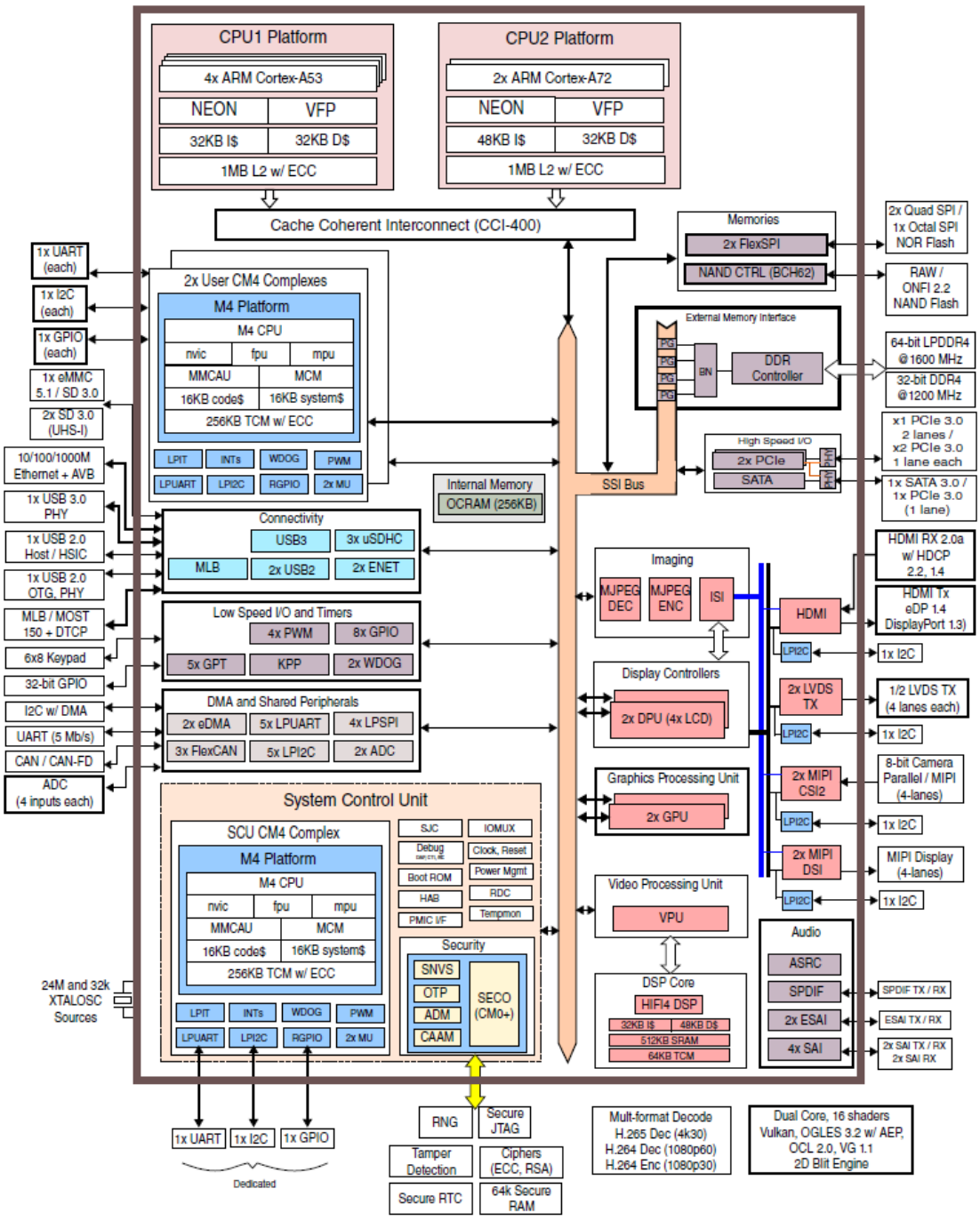


Figure 2 : iMX 8M Block Diagram

5.1.3 ARM Cortex-A53 MPCore™ Platform

The i.MX8QM family Applications Processors are based on the ARM Cortex-A53 MPCore™ platform, which has the following features:

- 4x cores
- L1 instruction cache 32K with parity
- L1 data cache 32K with SECDED
- Advanced SIMD (NEON) per core
- Crypto extension per core
- CPU cache protection per core
- AMBA 4 ACE interface
- 1MB of L2 Cache
  - 1M with SECDED
  - Input latency 2 cycles
  - Output latency 2 cycles
  - SCU-L2 cache protection

5.1.4 Arm Cortex A72 Platform

Cortex-A72 core platform includes the following features:

- 2x cores
- L1 instruction cache 48K with parity
- L1 data cache 32K
- Advanced SIMD (NEON) per core
- Crypto extension per core
- CPU cache protection per core
- AMBA 4 ACE interface
- 1MB of L2 Cache
- 1MB with ECC protection

5.1.5 Arm Cortex-M4 Platform

The Cortex-M4 implements the ARMv7- ME instruction set architecture (ISA) and adds significant capabilities with DSP and SIMD extensions. The ARM Cortex-M4 core provides additional general processing capability to the SoC with lower power and fast interrupt response time. The Cortex-M4 also includes a single-precision floating-point unit (FPU) and two 32-bit system bus interfaces.
The Cortex-M4 implementation includes two tightly coupled local memories, two cache memories connected to bus interfaces, 64-bit system bus interconnect, and supports a 32-byte cache line size.

- ARM Cortex M4 CPU processor, including:
  - AHB LMEM (Local Memory Controller) including controllers for TCM and cache memories
  - 256 KB TCM (128 KB TCMU, 128 KB TCML)
  - 16 KB Code Bus Cache
  - 16 KB System Bus Cache
  - ECC for TCM memories and parity for code and system caches
  - Integrated Nested Vector Interrupt Controller (NVIC)
  - Wakeup Interrupt Controller (WIC)
  - FPU (Floating Point Unit)
  - Core MPU (Memory Protection Unit)
  - Support for exclusive access on the system bus
  - MMCAU (Crypto Acceleration Unit)
  - MCM (Miscellaneous Control Module)16 KB L1 Instruction Cache

5.2 Memory

5.2.1 RAM

The SPEAR-MX8 is available with up to 8 GB of LPDDR4 memory capable of running up to 3200MTS.

5.2.2 Non-volatile Storage Memory

The SPEAR-MX8 is available with a non-volatile storage memory with optional densities.
It is used for Flash Disk purposes, O.S. run-time-image, Boot-loader and application/user data storage.
The SPEAR-MX8 can arrive with up to 128GB MLC eMMC

5.3 Audio (WM8904)

The WM8904 is a high performance ultra-low power stereo CODEC optimized for portable audio applications.
The device features stereo ground-referenced headphone amplifiers using the Wolfson 'Class-W' amplifier techniques. It incorporates an innovative dual-mode charge pump architecture - to optimize efficiency and power consumption during playback.
The ground-referenced headphone output eliminates AC coupling capacitors, and both outputs include common mode feedback paths to reject ground noise. Control sequences for audio path setup can be pre-loaded and executed by an integrated control write sequencer to reduce software driver development and minimize pops and clicks via SilentSwitch™ technology. The input impedance is constant with PGA gain setting. A stereo digital microphone interface is provided, with a choice of two inputs. A dynamic range controller provides compression and level control to support a wide range of portable recording applications. Anti-clip and quick release features offer good performance in the presence of loud impulsive noises. ReTuneTM Mobile 5-band parametric equalizer with fully programmable coefficients is integrated for optimization of speaker characteristics. Programmable dynamic range control is also available for maximizing loudness, protecting speakers from clipping and preventing premature shutdown due to battery droop. Common audio sampling frequencies are supported from a wide range of external clocks, either directly or generated via the FLL.

Features:

- 3.0mW quiescent power consumption for DAC to headphone playback
- DAC SNR 96dB typical, THD -86dB typical
- ADC SNR 91dB typical, THD -80dB typical
- 2.4mW quiescent power consumption for analogue bypass playback
- Control write sequencer for pop minimized start-up and shutdown
- Single register writes for default start-up sequence
- Integrated FLL provides all necessary clocks - Self-clocking modes allow processor to sleep - All standard sample rates from 8kHz to 96kHz
- Stereo digital microphone input
- 2 single ended inputs per stereo channel
- Digital Dynamic Range Controller (compressor / limiter)
- Digital sidetone mixing
- Ground-referenced headphone driver

5.4 Wi-Fi + BT (LWB5™)

The SPEAR-MX8 contains LSR's pre-certified high-performance Sterling-LWB5™ Dual band 2.4/5 GHz Wi-Fi® and Bluetooth® Smart Ready Multi-Standard Module based upon the Cypress (formerly Broadcom) CYW43353 chipset supporting 802.11 ac/a/b/g/n, BT 2.1+EDR, and BLE 5.2 wireless connectivity.

The SPEAR-MX8 module realizes the necessary PHY/MAC layers to support WLAN applications in conjunction with a host processor over a SDIO interface.
The modules also provide a Bluetooth/BLE platform through the HCI transport layer. Both WLAN and Bluetooth share the same antenna port.

Key Features:

- IEEE 802.11 ac/a/b/g/n
- Bluetooth 2.1+EDR, and BLE 5.2
- U.F.L connector for external antenna
- Latest Linux and Android drivers supported directly by LSR and Cypress
- Wi-Fi/BT module Broad certifications with multiple antennas: FCC (USA), IC (Canada), ETSI (Europe), Giteki (Japan), and RCM (AU/NZ)
- Industrial operating Temperature Range: -40 to +85
- Tristate buffer on the BT link based on UART interface will allow isolation from the LWB5 module and the use by external circuity via the SPEAR-MX8 connector. The tristate buffer controlled by QSPI1A_DATA0 line (alternate function GPIO4_IO26)

5.5 PMIC

The SPEAR-MX8 features Dual Freescale/NXP's PF8200 chips as a Power Management Integrated circuit (PMIC) designed specifically for use with NXP's i.MX8QM series of application processors. The PF8200 regulates all power rails required on SOM from a single power supply with 3.4V – 4.5V range.
The PMIC is fully programmable via the I2C interface and associated register map. Additional communication is provided by direct logic interfacing including interrupt, watchdog and reset.

5.6 Dual 10/100/1000 Mbps Ethernet Transceiver

The SPEAR-MX8 can be ordered with one or two Integrated Ethernet Transceivers, Qualcomm Atheros AR8033 or Analog Devices ADIN1300.
Please contact sales@variscite.com for inquiries about P/N assembled on your SOM.

5.6.1 Qualcomm Atheros AR8033 Ethernet Transceiver

Key features include:

- 10BASE-Te/100BASE-TX/1000BASE-T IEEE 802.3 compliant
- 1000BASE-T PCS and auto-negotiation with next page support
- Green ETHOS power saving modes with internal automatic DSP power saving scheme
- IEEE 802.3az EEE
- Fully integrated digital adaptive equalizers, echo cancellers, and Near End Crosstalk (NEXT) cancellers
- Robust Cable Discharge Event (CDE) protection of ±6 kV
- Robust operation over up to 140 meters of CAT5 cable

- Automatic Channel Swap (ACS)
- Automatic MDI/MDIX crossover
- Automatic polarity correction ν IEEE 802.3u compliant auto-negotiation
- Jumbo frame supports up to 10 KB (full-duplex)
- Integrated termination circuitry at the line side

5.6.2 Analog Devices ADIN1300 Ethernet Transceiver

Key features include:

- 10BASE-Te/100BASE-TX/1000BASE-T IEEE® 802.3™ compliant MII, RMII, and RGMII MAC interfaces
- EEE in accordance with IEEE 802.3az
- Start of packet detection for IEEE 1588 time stamp support
- Enhanced link detection
- Configurable LED
- Integrated power supply monitoring and POR
- MII management interface (MDIO) compatible with the IEEE 802.3 Standard Clause 22 and Clause 45 management frame structures.
- Supports cable lengths up to 150 meters at Gigabit speeds and 180 meters when operating at 100 Mbps or 10 Mbps.
- Automatic MDI/MDIX crossover
- Autonegotiation capability in accordance with IEE 802.3 Clause 28
- Supports a number of power-down modes: hardware, software, and energy detect power-down, and EEE LPI mode
- On-chip cable diagnostics capabilities
- Transmit drivers are voltage mode with on-chip terminations

5.7 EEPROM

The SPEAR-MX8 uses 4Kbit serial EEPROM to store memory calibration and manufacturing parameters.
This EEPROM is connected to SCU I2C bus and intended only for holding the above information.
The SOM may not boot if the contents of EEPROM device is corrupted.

6 SPEAR-MX8 Hardware Configuration

SPEAR-MX8 hardware interfaces, explained on sections 5.3, 5.4 and 5.6, configured using the orderable part number of the module.

Table 2 details the part of the hardware configuration orderable options.

Table 2: Partial Hardware Configuration Options

Option	Description
EC	Dual Ethernet PHY assembled on SOM
AC	Audio Codec assembled on SOM
WBD	Dual band Wi-Fi and BT/BLE combo assembled on SOM

Note: Other orderable options are available and are not part of this datasheet.
Please refer to Variscite official website for full list of configuration options.

7 External Connectors

7.1 Board to Board Connector

- The SPEAR-MX8 exposes four 90-pin board-to-board connectors.
- The recommended mating connector is: Hirose Electric Co Ltd **PN: DF40C-90DS-0.4V(51)**

7.2 Wi-Fi & BT Connector

- Modules with Wi-Fi ***"WBD" Configuration*** **-** a combined Wi-Fi + BT antenna connector is assembled
- Connector type: **U.FL JACK connector**
- Cable and antenna shall have a 50 Ohm characteristic impedance

7.3 SPEAR-MX8 Connector Pin-out

Table 3: SPEAR-MX8 J1 Pinout

Pin #	Pin Name	GPIO	Voltage	Ball
J1.1	GPT0_COMPARE	GPIO0_IO16	3.3V	AW53
J1.2[1]	UART1_TX	GPIO0_IO24	3.3V	AY48
J1.3	GPT1_CAPTURE	GPIO0_IO18	3.3V	AY50
J1.4[1]	UART1_CTS_B	GPIO0_IO27	3.3V	AV46
J1.5	GPT1_CLK	GPIO0_IO17	3.3V	BA53
J1.6[1]	UART1_RTS_B	GPIO0_IO26	3.3V	AR43
J1.7	GPT1_COMPARE	GPIO0_IO19	3.3V	BA51
J1.8[1]	UART1_RX	GPIO0_IO25	3.3V	AT44
J1.9	M41_I2C0_SCL	GPIO0_IO10	3.3V	AR45
J1.10	UART0_TX	GPIO0_IO21	3.3V	AV48
J1.11	M41_GPIO0_IO01	GPIO0_IO13	3.3V	AU47
J1.12	UART0_CTS_B	GPIO0_IO23	3.3V	AW49
J1.13	GND		3.3V	
J1.14	UART0_RTS_B	GPIO0_IO22	3.3V	AU45
J1.15	SCU_DSC_BOOT_MODE2		1.8V	BJ53
J1.16	UART0_RX	GPIO0_IO20	3.3V	AV50
J1.17	SCU_DSC_BOOT_MODE3		1.8V	BA43
J1.18	GND		3.3V	
J1.19	SCU_DSC_BOOT_MODE5		1.8V	BK52
J1.20[4]	MIPI_DSI0_CLK_N		3.3V	BN27
J1.21	SNVS_ON_OFF_BUTTON		1.8V	BE47
J1.22[4]	MIPI_DSI0_CLK_P		3.3V	BL27
J1.23	SCU_GPIO0_IO01	GPIO0_IO29	1.8V	AV44
J1.24	GND		3.3V	

Pin #	Pin Name	GPIO	Voltage	Ball
J1.25	SCU_GPIO0_IO00	GPIO0_IO28	1.8V	AU43
J1.26[4]	MIPI_DSI0_DATA0_P		3.3V	BK28
J1.27	SCU_GPIO0_IO05	GPIO1_IO01	1.8V	AY44
J1.28[4]	MIPI_DSI0_DATA0_N		3.3V	BM28
J1.29	SCU_GPIO0_IO06	GPIO1_IO02	1.8V	BG49
J1.30[4]	MIPI_DSI0_DATA1_P			BK26
J1.31	SNVS_TAMPER_OUT0		1.8V	BD46
J1.32[4]	MIPI_DSI0_DATA1_N			BM26
J1.33	SNVS_TAMPER_OUT1		1.8V	BD42
J1.34[4]	MIPI_DSI0_DATA2_P			BL29
J1.35	SNVS_TAMPER_IN0		1.8V	BE41
J1.36[4]	MIPI_DSI0_DATA2_N			BN29
J1.37	SNVS_TAMPER_IN1		1.8V	BE43
J1.38[4]	MIPI_DSI0_DATA3_P			BL25
J1.39	GND		3.3V	
J1.40[4]	MIPI_DSI0_DATA3_N			BN25
J1.41	LVDS0_T0DP			BN45
J1.42	GND			
J1.43	LVDS0_T0DN			BL45
J1.44	LVDS1_T0CLKP			BM36
J1.45	LVDS0_T0CP			BM44
J1.46	LVDS1_T0CLKN			BK36
J1.47	LVDS0_T0CN			BK44
J1.48	GND			
J1.49	LVDS0_T0BP			BN43
J1.50	LVDS1_T0AP			BN37
J1.51	LVDS0_T0BN			BL43
J1.52	LVDS1_T0AN			BL37
J1.53	LVDS0_T0AP			BM42
J1.54	LVDS1_T0BP			BM38
J1.55	LVDS0_T0AN			BK42
J1.56	LVDS1_T0BN			BK38
J1.57	GND			
J1.58	LVDS1_T0CP			BN39
J1.59	LVDS0_T0CLKP			BN41
J1.60	LVDS1_T0CN			BL39
J1.61	LVDS0_T0CLKN			BL41
J1.62	LVDS1_T0DP			BM40
J1.63	GND			

Pin #	Pin Name	GPIO	Voltage	Ball
J1.64	LVDS1_T0DN			BK40
J1.65	LVDS0_T1DP			BH38
J1.66	GND			
J1.67	LVDS0_T1DN			BG37
J1.68[4]	MIPI_DSI0_I2C0_SDA	GPIO1_IO17	3.3V	BE31
J1.69	LVDS0_T1CP			BH40
J1.70[4]	MIPI_DSI0_I2C0_SCL	GPIO1_IO16	3.3V	BE29
J1.71	LVDS0_T1CN			BG39
J1.72	LVDS1_I2C0_SDA	GPIO1_IO13	3.3V	BE33
J1.73	LVDS0_T1BP			BH42
J1.74	LVDS1_I2C0_SCL	GPIO1_IO12	3.3V	BL35
J1.75	LVDS0_T1BN			BG41
J1.76[4]	MIPI_DSI0_GPIO0_00	GPIO1_IO18	3.3V	BD30
J1.77	LVDS0_T1AP			BH44
J1.78[4]	MIPI_DSI0_GPIO0_01	GPIO1_IO19	3.3V	BD28
J1.79	LVDS0_T1AN			BG43
J1.80	LVDS0_I2C1_SDA	GPIO1_IO09	3.3V	BE35
J1.81	GND			
J1.82	LVDS0_I2C1_SCL	GPIO1_IO08	3.3V	BE37
J1.83	LVDS0_T1CLKP			BH46
J1.84	LVDS0_I2C0_SDA	GPIO1_IO07	3.3V	BD36
J1.85	LVDS0_T1CLKN			BG45
J1.86	LVDS0_I2C0_SCL	GPIO1_IO06	3.3V	BD38
J1.87	GND			
J1.88	GND			
J1.89	LVDS0_GPIO0_IO00	GPIO1_IO04	3.3V	BE39
J1.90	LVDS0_GPIO0_IO01	GPIO1_IO05	3.3V	BD40

Note [1]: Signals are shared with the On-SOM Bluetooth.
Note [4]: DSI0 interface is not accessible when LVDS option is assembled.

Table 4: SPEAR-MX8 J2 Pinout

Pin #	Pin Name	GPIO	Voltage	Ball
J2.1	NC (Removed HDMI_RX0_RX_P_LN_2)			BM20
J2.2	MIPI_CSI0_ACM_MCLK_OUT	GPIO1_IO24	1.8V	BJ23
J2.3	NC (Removed HDMI_RX0_RX_M_LN_2)			BL19
J2.4	MIPI_CSI1_ACM_MCLK_OUT	GPIO1_IO29	1.8V	BN23
J2.5	NC (Removed HDMI_RX0_RX_P_LN_1)			BM18
J2.6	MIPI_CSI0_I2C0_SCL	GPIO1_IO25	1.8V	BH24
J2.7	NC (Removed HDMI_RX0_RX_M_LN_1)			BL17
J2.8	MIPI_CSI1_I2C0_SDA	GPIO2_IO01	1.8V	BE15
J2.9	NC (Removed HDMI_RX0_RX_P_LN_0)			BM16
J2.10	MIPI_CSI0_GPIO0_IO00	GPIO1_IO27	1.8V	BL23
J2.11	NC (Removed HDMI_RX0_RX_M_LN_0)			BL15
J2.12	MIPI_CSI0_GPIO0_IO01	GPIO1_IO28	1.8V	BM22
J2.13	NC (Removed HDMI_RX0_ARC_P)			BM14
J2.14	MIPI_CSI0_I2C0_SDA	GPIO1_IO26	1.8V	BN19
J2.15	NC (Removed HDMI_RX0_ARC_M)			BL13
J2.16	MIPI_CSI1_I2C0_SCL	GPIO2_IO00	1.8V	BN17
J2.17	GND			
J2.18	MIPI_CSI1_GPIO0_IO00	GPIO1_IO30	1.8V	BN15
J2.19	NC (Removed HDMI_RX0_RX_CLK_P)			BM12
J2.20	MIPI_CSI1_GPIO0_IO01	GPIO1_IO31	1.8V	BN13
J2.21	NC (Removed HDMI_RX0_RX_CLK_M)			BL11
J2.22	GND			
J2.23	GND			
J2.24	MIPI_CSI1_CKP			BJ17
J2.25	NC (Removed HDMI_RX0_CEC)		3.3V	BJ9
J2.26	MIPI_CSI1_CKN			BH16
J2.27	NC (Removed HDMI_RX0_HPD)		3.3V	BF14
J2.28	GND			
J2.29	NC (Removed HDMI_RX0_DDC_SDA)		3.3V	BE13
J2.30	MIPI_CSI1_DP0			BJ19
J2.31	NC (Removed HDMI_RX0_DDC_SCL)		3.3V	BH10
J2.32	MIPI_CSI1_DN0			BH18
J2.33	NC (Removed HDMI_RX0_MON_5V)		3.3V	BN11
J2.34	MIPI_CSI1_DP1			BJ15
J2.35	GND		3.3V	
J2.36	MIPI_CSI1_DN1			BH14
J2.37	HDMI_TX0_TX_P_LN_0		3.3V	BL9
J2.38	MIPI_CSI1_DP2			BJ21

Pin #	Pin Name	GPIO	Voltage	Ball
J2.39	HDMI_TX0_TX_M_LN_0			BM8
J2.40	MIPI_CSI1_DN2			BH20
J2.41	HDMI_TX0_TX_P_LN_1			BL7
J2.42	MIPI_CSI1_DP3			BJ13
J2.43	HDMI_TX0_TX_M_LN_1			BM6
J2.44	MIPI_CSI1_DN3			BH12
J2.45	HDMI_TX0_TX_P_LN_2			BL5
J2.46	GND			
J2.47	HDMI_TX0_TX_M_LN_2			BM4
J2.48	MIPI_CSI0_CKP			BF20
J2.49	HDMI_TX0_AUX_P			BH2
J2.50	MIPI_CSI0_CKN			BE21
J2.51	HDMI_TX0_AUX_M			BG3
J2.52	GND			
J2.53	GND			
J2.54	MIPI_CSI0_DP0			BF22
J2.55	HDMI_TX0_TX_P_LN_3			BL3
J2.56	MIPI_CSI0_DN0			BE23
J2.57	HDMI_TX0_TX_M_LN_3			BK2
J2.58	MIPI_CSI0_DP1			BF18
J2.59	GND			
J2.60	MIPI_CSI0_DN1			BE19
J2.61	HDMI_TX0_CEC		3.3V	BJ1
J2.62	MIPI_CSI0_DP2			BF24
J2.63	HDMI_TX0_HPD		3.3V	BH8
J2.64	MIPI_CSI0_DN2			BE25
J2.65	HDMI_TX0_DDC_SDA		3.3V	BN5
J2.66	MIPI_CSI0_DP3			BF16
J2.67	HDMI_TX0_DDC_SCL		3.3V	BG1
J2.68	MIPI_CSI0_DN3			BE17
J2.69	GND			
J2.70	GND			
J2.71	SAI1_RXD	GPIO3_IO13	3.3V	AV4
J2.72	SPI0_SDI	GPIO3_IO04	3.3V	BA5
J2.73	SAI1_TXFS	GPIO3_IO17	3.3V	AV2
J2.74	SPI0_SCK	GPIO3_IO02	3.3V	BB4
J2.75	SPI2_CS0	GPIO3_IO10	3.3V	AW1
J2.76	SPI0_SDO	GPIO3_IO03	3.3V	AY6
J2.77	SPI2_SDO	GPIO3_IO08	3.3V	BA1

Pin #	Pin Name	GPIO	Voltage	Ball
J2.78	SPI0_CS0	GPIO3_IO05	3.3V	BC1
J2.79	ESAI1_TX0	GPIO2_IO08	3.3V	BF10
J2.80	SPI0_CS1	GPIO3_IO06	3.3V	BA3
J2.81	ESAI1_FSR	GPIO2_IO04	3.3V	BE11
J2.82	SPI3_SDO	GPIO2_IO18	3.3V	BF2
J2.83	ESAI1_SCKR	GPIO2_IO06	3.3V	BD12
J2.84	SPI3_CS0	GPIO2_IO20	3.3V	BG5
J2.85	ESAI1_FST	GPIO2_IO05	3.3V	BF12
J2.86	SPI3_SCK	GPIO2_IO17	3.3V	BF6
J2.87	ACM_MCLK_IN0	GPIO3_IO00	3.3V	BC3
J2.88	HDMI_TX0_I2C0_SCL	GPIO2_IO02	3.3V	BN9
J2.89	SPI2_CS1	GPIO3_IO11	3.3V	AY2
J2.90	HDMI_TX0_I2C0_SDA	GPIO2_IO03	3.3V	BN7

Table 5: SPEAR-MX8 J3 Pinout

Pin #	Pin Name	GPIO	Voltage	Ball
J3.1	ETH0_MDI_A_P			AR8033.11/ ADIN1300.12
J3.2[2]	ETH1_MDI_A_P(ENET1_RGMII_TXD0)	(GPIO6_IO12)	(3.3V/1.8V)	AR8033.11/ ADIN1300.12 (A49)
J3.3	ETH0_MDI_A_M			AR8033.12/ ADIN1300.13
J3.4[2]	ETH1_MDI_A_M(ENET1_RGMII_RXD2)	(GPIO6_IO20)	(3.3V/1.8V)	AR8033.12/ ADIN1300.13 (D52)
J3.5	ETH0_MDI_B_P			AR8033.14/ ADIN1300.14
J3.6[2]	ETH1_MDI_B_P(ENET1_RGMII_RXD3)	(GPIO6_IO21)	(3.3V/1.8V)	AR8033.14/ ADIN1300.14 (E53)
J3.7	ETH0_MDI_B_M			AR8033.15/ ADIN1300.15
J3.8[2]	ETH1_MDI_B_M(ENET1_RGMII_TXD1)	(GPIO6_IO13)	(3.3V/1.8V)	AR8033.15/ ADIN1300.15 (C47)
J3.9	ETH0_MDI_C_P			AR8033.17/ ADIN1300.16
J3.10[2]	ETH1_MDI_C_P(ENET1_RGMII_RXC)	(GPIO6_IO16)	(3.3V/1.8V)	AR8033.17/ ADIN1300.16 (B50)
J3.11	ETH0_MDI_C_M			AR8033.18/ ADIN1300.17
J3.12[2]	ETH1_MDI_C_M(ENET1_RGMII_RX_CTL)	(GPIO6_IO17)	(3.3V/1.8V)	AR8033.18/ ADIN1300.17 (E49)
J3.13	ETH0_MDI_D_P			AR8033.20/ ADIN1300.18
J3.14[2]	ETH1_MDI_D_P(ENET1_RGMII_RXD0)	(GPIO6_IO18)	(3.3V/1.8V)	AR8033.20/ ADIN1300.18 (E51)
J3.15	ETH0_MDI_D_M			AR8033.21/ ADIN1300.19
J3.16[2]	ETH1_MDI_D_M(ENET1_RGMII_RXD1)	(GPIO6_IO19)	(3.3V/1.8V)	AR8033.21/ ADIN1300.19 (C51)
J3.17	ETH0_LED_ACT			AR8033.23/ ADIN1300.21 (via inv. FET)
J3.18[2]	ETH1_LED_ACT(ENET1_RGMII_TX_CTL)	(GPIO6_IO11)	(3.3V/1.8V)	AR8033.23/ ADIN1300.21 (via inv. FET) (B48)
J3.19	ETH0_LED_LINK_1000		3.3V	AR8033.24/ ADIN1300.26 (via level shifter)
J3.20[2]	ETH1_LED_LINK_1000(ENET1_RGMII_TXD2)	(GPIO6_IO14)	(3.3V/1.8V)	AR8033.24/ ADIN1300.26 (via level shifter) (G47)
J3.21	ETH0_LED_LINK_10_100		3.3V	AR8033.26/ ADIN1300-GND
J3.22[2]	ETH1_LED_LINK_10_100(ENET1_RGMII_TXC)	(GPIO6_IO10)	(3.3V/1.8V)	AR8033.26/ ADIN1300-GND (D46)
J3.23[6]	ENET0_MDC	GPIO4_IO14	3.3V	A9
J3.24[6]	ENET0_MDIO	GPIO4_IO13	3.3V	D10
J3.25	USB_OTG2_ID		3.3V	F30
J3.26	GPT0_CAPTURE	GPIO0_IO15	3.3V	AV52
J3.27	GND			
J3.28	GND			

Pin #	Pin Name	GPIO	Voltage	Ball
J3.29	M40_GPIO0_IO01	GPIO0_IO09	3.3V	AU53
J3.30	GPT0_CLK	GPIO0_IO14	3.3V	AY52
J3.31[2]	NC(ENET1_RGMII_TXD3)	(GPIO6_IO15)	(3.3V)	(D48)
J3.32	M40_I2C0_SDA	GPIO0_IO07	3.3V	AU51
J3.33	USDHC1_DATA6	GPIO5_IO21	LDO_SD1	F42
J3.34	M40_GPIO0_IO00	GPIO0_IO08	3.3V	AR47
J3.35	USDHC1_DATA5	GPIO5_IO20	LDO_SD1	G43
J3.36	M41_I2C0_SDA	GPIO0_IO11	3.3V	AU49
J3.37	USDHC1_CMD	GPIO5_IO14	LDO_SD1	G41
J3.38	M40_I2C0_SCL	GPIO0_IO06	3.3V	AM44
J3.39	USDHC1_DATA4	GPIO5_IO19	LDO_SD1	H40
J3.40	M41_GPIO0_IO00	GPIO0_IO12	3.3V	AP44
J3.41	USDHC1_DATA3	GPIO5_IO18	LDO_SD1	F40
J3.42	USDHC1_STROBE	GPIO5_IO23	LDO_SD1	J43
J3.43	USDHC1_DATA2	GPIO5_IO17	LDO_SD1	E39
J3.44	USDHC1_DATA7	GPIO5_IO22	LDO_SD1	H42
J3.45	USDHC1_DATA1	GPIO5_IO16	LDO_SD1	F38
J3.46	USB_OTG1_DP			B40
J3.47	USDHC1_DATA0	GPIO5_IO15	LDO_SD1	E37
J3.48	USB_OTG1_DN			C39
J3.49	USDHC1_CLK		LDO_SD1	J39
J3.50	GND			
J3.51	GND			
J3.52	USB_OTG2_DP			B38
J3.53	USB_OTG1_VBUS		3.3V	A39
J3.54	USB_OTG2_DM			C37
J3.55	USB_OTG1_ID		3.3V	A37
J3.56	GND			
J3.57	USB_OTG2_VBUS		3.3V	A35
J3.58	USB_SS3_RX_P_LN_0			C35
J3.59	GND			
J3.60	USB_SS3_RX_M_LN_0			B34
J3.61	SNVS_PMIC_ON_REQ		1.8V	BL51
J3.62	GND			
J3.63	SCU_WDOG0_WDOG_OUT		1.8V	BB50
J3.64	USB_SS3_TX_P_LN_0			A33
J3.65	POR_B_1V8		1.8V	BE49
J3.66	USB_SS3_TX_M_LN_0			B32
J3.67	SW_3P3			

Pin #	Pin Name	GPIO	Voltage	Ball
J3.68	SW_1P8			
J3.69	VBAT			
J3.70	VBAT			
J3.71	VBAT			
J3.72	VBAT			
J3.73	VBAT			
J3.74	VBAT			
J3.75	VBAT			
J3.76	VBAT			
J3.77	VBAT			
J3.78	VBAT			
J3.79	VBAT			
J3.80	VBAT			
J3.81	VBAT			
J3.82	VBAT			
J3.83	VBAT			
J3.84	VBAT			
J3.85	VBAT			
J3.86	VBAT			
J3.87	VBAT			
J3.88	VBAT			
J3.89	VBAT			
J3.90	VBAT			

Note [2]: There is an assembly option to expose RGMII interface.
Voltage Level of these pins on SOM PCB Revisions up to 1.3 is 3.3V.
ON PCB Revisions 1.3 and up, RGMII Interface can be 3.3V (By default) or 1.8V.
The selection is done using GPIO2_IO27.
Low level of this GPIO will select 3.3V, high level will select 1.8V.

Note [6]: The pin mode cannot be changed on SOMs that have at least one Ethernet PHY assembled.

Table 6: SPEAR-MX8 J4 Pinout

Pin #	Pin Name	GPIO	Voltage	Ball
J4.1	LDO_SD1			
J4.2	HSIO_PCIE_IOB_EXT_REFCLK100M_N			E25
J4.3	GND			
J4.4	HSIO_PCIE_IOB_EXT_REFCLK100M_P			F26
J4.5	HSIO_PCIE1_CLKREQ_B	GPIO4_IO30	3.3V	A25
J4.6	GND			
J4.7	HSIO_PCIE0_WAKE_B	GPIO4_IO28	3.3V	A15
J4.8	HSIO_PCIE0_RX0_P			A29
J4.9	HSIO_PCIE1_WAKE_B	GPIO4_IO31	3.3V	A27
J4.10	HSIO_PCIE0_RX0_N			B30
J4.11	HSIO_PCIE0_CLKREQ_B	GPIO4_IO27	3.3V	A17
J4.12	GND			
J4.13	HSIO_PCIE0_PERST_B	GPIO4_IO29	3.3V	D20
J4.14	HSIO_PCIE0_TX0_P			B26
J4.15	HSIO_PCIE1_PERST_B	GPIO5_IO00	3.3V	G25
J4.16	HSIO_PCIE0_TX0_N			C27
J4.17	GND			
J4.18	GND			
J4.19[5]	VCC_HSIC			V26
J4.20	HSIO_PCIE2_RX0_P			A19
J4.21[5]	USB_HSIC0_STROBE	GPIO5_IO02	VCC_HSIC	F28
J4.22	HSIO_PCIE2_RX0_N			B20
J4.23[5]	USB_HSIC0_DATA	GPIO5_IO01	VCC_HSIC	H26
J4.24	GND			
J4.25	GND			
J4.26	HSIO_PCIE2_TX0_P			B16
J4.27	ESAI1_TX4_RX1	GPIO2_IO12	3.3V	AY12
J4.28	HSIO_PCIE2_TX0_N			C17
J4.29	VCOIN			
J4.30	GND			
J4.31	SAI1_RXFS	GPIO3_IO14	3.3V	AU3
J4.32	SPDIF0_TX	GPIO2_IO15	3.3V	BC9
J4.33	GND			
J4.34	SPI3_CS1	GPIO2_IO21	3.3V	BD8
J4.35	USDHC1_RESET_B	GPIO4_IO07	LDO_SD1	A5
J4.36	SPDIF0_RX	GPIO2_IO14	3.3V	BC7
J4.37	ESAI1_TX1	GPIO2_IO09	3.3V	BA11
J4.38	SPDIF0_EXT_CLK	GPIO2_IO16	3.3V	BD6

Pin #	Pin Name	GPIO	Voltage	Ball
J4.39	GND			
J4.40	SPI3_SDI	GPIO2_IO19	3.3V	BE5
J4.41	GND			
J4.42	SPI2_SDI	GPIO3_IO09	3.3V	AY4
J4.43	ESAI1_TX2_RX3	GPIO2_IO10	3.3V	AU11
J4.44	SAI1_TXD	GPIO3_IO16	3.3V	AU1
J4.45	ESAI1_TX3_RX2	GPIO2_IO11	3.3V	AV10
J4.46	ESAI1_SCKT	GPIO2_IO07	3.3V	AY10
J4.47[7]	MLB_CLK	GPIO3_IO27	3.3V	D2
J4.48	P2_LDO4			PF8100VAA0ES-2.28
J4.49	GND			
J4.50	P2_LDO4			PF8100VAA0ES-2.28
J4.51	ENET1_REFCLK_125M_25M	GPIO4_IO16	3.3V	A11
J4.52	P2_LDO3			PF8100VAA0ES-2.25
J4.53	ENET0_REFCLK_125M_25M	GPIO4_IO15	3.3V	B10
J4.54	P2_LDO3			PF8100VAA0ES-2.25
J4.55	I2C1_SDA	GPIO4_IO06	3.3V	H10
J4.56	ESAI1_TX5_RX0	GPIO2_IO13	3.3V	AT10
J4.57	I2C1_SDA	GPIO4_IO05	3.3V	F8
J4.58	ADC_IN1	GPIO3_IO19	1.8V	AN11
J4.59	FLEXCAN2_RX	GPIO4_IO01	3.3V	C3
J4.60	ADC_IN0	GPIO3_IO18	1.8V	AP10
J4.61	FLEXCAN2_TX	GPIO4_IO02	3.3V	E7
J4.62	ADC_IN6	GPIO3_IO24	1.8V	AL9
J4.63	I2C1_SCL	GPIO4_IO04	3.3V	L9
J4.64	ADC_IN4	GPIO3_IO22	1.8V	AN9
J4.65	I2C1_SCL	GPIO4_IO03	3.3V	J9
J4.66	ADC_IN5	GPIO3_IO23	1.8V	AR7
J4.67	SAI1_TXC	GPIO3_IO15	3.3V	AU5
J4.68	ADC_IN3	GPIO3_IO21	1.8V	AR9
J4.69	SAI1_RXC	GPIO3_IO12	3.3V	AV6
J4.70	ADC_IN7	GPIO3_IO25	1.8V	AP6
J4.71	SPI2_SCK	GPIO3_IO07	3.3V	AW5
J4.72	ADC_IN2	GPIO3_IO20	1.8V	AP8
J4.73[3]	ENET1_MDC	GPIO4_IO18	3.3V	A13
J4.74	FLEXCAN1_RX	GPIO3_IO31	3.3V	E5
J4.75[3]	ENET1_MDIO	GPIO4_IO17	3.3V	C13
J4.76	FLEXCAN1_TX	GPIO4_IO00	3.3V	G7
J4.77	GND			

Pin #	Pin Name	GPIO	Voltage	Ball
J4.78	GND			
J4.79	FLEXCAN0_RX	GPIO3_IO29	3.3V	C5
J4.80	FLEXCAN0_TX	GPIO3_IO30	3.3V	H6
J4.81	DMIC_CLK		1.8V	WM8904CGEFL.1
J4.82[7]	MLB_DATA	GPIO3_IO28	3.3V	E3
J4.83	DMIC_DATA		1.8V	WM8904CGEFL.27
J4.84[7]	MLB_SIG	GPIO3_IO26	3.3V	E1
J4.85	HPLOUT		3.3V	WM8904CGEFL.13
J4.86	LINEIN1_RP		3.3V	WM8904CGEFL.24
J4.87	HPROUT		3.3V	WM8904CGEFL.15
J4.88	LINEIN1_LP		3.3V	WM8904CGEFL.26
J4.89	HPOUTFB		3.3V	WM8904CGEFL.14
J4.90	AGND			WM8904CGEFL.22

Note [3]: I2C4 interface is used by CODEC on the SOM
Pin configuration for I2C4 signal can't be changed.
Note [5]: VCC_HSIC should be 1.2V if HSIC interface is in use.
Note [7]: MLB Interface was removed. Do not use.

Table 7: SPEAR-MX8 PINMUX

Pin #	Alt 0	Alt 1	Alt 2	Alt 3
J1.1	GPT0_COMPARE	PWM3_OUT	KPP0_COL6	GPIO0_IO16
J1.2[1]	UART1_TX	SPI3_SCK		GPIO0_IO24
J1.3	GPT1_CAPTURE	I2C2_SDA	KPP0_ROW4	GPIO0_IO18
J1.4[1]	UART1_CTS_B	SPI3_CS0	UART1_RTS_B	GPIO0_IO27
J1.5	GPT1_CLK	I2C2_SCL	KPP0_COL7	GPIO0_IO17
J1.6[1]	UART1_RTS_B	SPI3_SDI	UART1_CTS_B	GPIO0_IO26
J1.7	GPT1_COMPARE	PWM2_OUT	KPP0_ROW5	GPIO0_IO19
J1.8[1]	UART1_RX	SPI3_SDO		GPIO0_IO25
J1.9	M41_I2C0_SCL	M41_UART0_RX	M41_GPIO0_IO02	GPIO0_IO10
J1.10	UART0_TX			GPIO0_IO21
J1.11	M41_GPIO0_IO01	M41_TPM0_CH1	UART3_TX	GPIO0_IO13
J1.12	UART0_CTS_B	PWM1_OUT	UART2_TX	GPIO0_IO23
J1.14	UART0_RTS_B	PWM0_OUT	UART2_RX	GPIO0_IO22
J1.16	UART0_RX			GPIO0_IO20
J1.23	SCU_GPIO0_IO01	SCU_UART0_TX		GPIO0_IO29
J1.25	SCU_GPIO0_IO00	SCU_UART0_RX		GPIO0_IO28
J1.27	SCU_GPIO0_IO05	SCU_GPIO0_IOXX_PMIC_A53_ON		GPIO1_IO01
J1.29	SCU_GPIO0_IO06	SCU_TPM0_CH0		GPIO1_IO02
J1.68[4]	MIPI_DSI0_I2C0_SDA			GPIO1_IO17
J1.70[4]	MIPI_DSI0_I2C0_SCL			GPIO1_IO16
J1.72	LVDS1_I2C0_SDA	LVDS1_GPIO0_IO03		GPIO1_IO13
J1.74	LVDS1_I2C0_SCL	LVDS1_GPIO0_IO02		GPIO1_IO12
J1.76[4]	MIPI_DSI0_GPIO0_IO00	MIPI_DSI0_PWM0_OUT		GPIO1_IO18
J1.78[4]	MIPI_DSI0_GPIO0_IO01			GPIO1_IO19
J1.80	LVDS0_I2C1_SDA	UART2_RX		GPIO1_IO09
J1.82	LVDS0_I2C1_SCL	UART2_TX		GPIO1_IO08
J1.84	LVDS0_I2C0_SDA	LVDS0_GPIO0_IO03		GPIO1_IO07
J1.86	LVDS0_I2C0_SCL	LVDS0_GPIO0_IO02		GPIO1_IO06
J1.89	LVDS0_GPIO0_IO00	LVDS0_PWM0_OUT		GPIO1_IO04
J1.90	LVDS0_GPIO0_IO01			GPIO1_IO05
J2.2	MIPI_CSI0_ACM_MCLK_OUT			GPIO1_IO24
J2.4	MIPI_CSI1_ACM_MCLK_OUT			GPIO1_IO29
J2.6	MIPI_CSI0_I2C0_SCL			GPIO1_IO25
J2.8	MIPI_CSI1_I2C0_SDA			GPIO2_IO01
J2.10	MIPI_CSI0_GPIO0_IO00	I2C0_SCL		GPIO1_IO27
J2.12	MIPI_CSI0_GPIO0_IO01	I2C0_SDA		GPIO1_IO28
J2.14	MIPI_CSI0_I2C0_SDA			GPIO1_IO26
J2.16	MIPI_CSI1_I2C0_SCL			GPIO2_IO00

Pin #	Alt 0	Alt 1	Alt 2	Alt 3
J2.18	MIPI_CSI1_GPIO0_IO00	UART4_RX		GPIO1_IO30
J2.20	MIPI_CSI1_GPIO0_IO01	UART4_TX		GPIO1_IO31
J2.71	SAI1_RXD	SAI0_TXFS		GPIO3_IO13
J2.72	SPI0_SDI	SAI0_RXD		GPIO3_IO04
J2.73	SAI1_TXFS	SAI1_RXFS		GPIO3_IO17
J2.74	SPI0_SCK	SAI0_RXC		GPIO3_IO02
J2.75	SPI2_CS0			GPIO3_IO10
J2.76	SPI0_SDO	SAI0_TXD		GPIO3_IO03
J2.77	SPI2_SDO			GPIO3_IO08
J2.78	SPI0_CS0	SAI0_RXFS		GPIO3_IO05
J2.79	ESAI1_TX0	SAI2_RXD		GPIO2_IO08
J2.80	SPI0_CS1	SAI0_TXC		GPIO3_IO06
J2.81	ESAI1_FSR			GPIO2_IO04
J2.82	SPI3_SDO	FTM_CH0		GPIO2_IO18
J2.83	ESAI1_SCKR			GPIO2_IO06
J2.84	SPI3_CS0	FTM_CH2		GPIO2_IO20
J2.85	ESAI1_FST			GPIO2_IO05
J2.86	SPI3_SCK			GPIO2_IO17
J2.87	ACM_MCLK_IN0	ESAI0_RX_HF_CLK		GPIO3_IO00
J2.88	HDMI_TX0_I2C0_SCL	I2C0_SCL		GPIO2_IO02
J2.89	SPI2_CS1	SAI0_TXFS		GPIO3_IO11
J2.90	HDMI_TX0_I2C0_SDA	I2C0_SDA		GPIO2_IO03
J3.2[2]	ENET1_RGMII_TXD0			GPIO6_IO12
J3.4[2]	ENET1_RGMII_RXD2	ENET1_RMII_RX_ER	TSI_S0_CLK	GPIO6_IO20
J3.6[2]	ENET1_RGMII_RXD3	UART3_RX	TSI_S1_CLK	GPIO6_IO21
J3.8[2]	ENET1_RGMII_TXD1			GPIO6_IO13
J3.10[2]	ENET1_RGMII_RXC	UART3_CTS_B	TSI_S1_DATA	GPIO6_IO16
J3.12[2]	ENET1_RGMII_RX_CTL		TSI_S0_VID	GPIO6_IO17
J3.14[2]	ENET1_RGMII_RXD0		TSI_S0_SYNC	GPIO6_IO18
J3.16[2]	ENET1_RGMII_RXD1		TSI_S0_DATA	GPIO6_IO19
J3.18[2]	ENET1_RGMII_TX_CTL			GPIO6_IO11
J3.20[2]	ENET1_RGMII_TXD2	UART3_TX	TSI_S1_VID	GPIO6_IO14
J3.22[2]	ENET1_RGMII_TXC	ENET1_RCLK50M_OUT	ENET1_RCLK50M_IN	GPIO6_IO10
J3.23[6]	ENET0_MDC	I2C4_SCL		GPIO4_IO14
J3.24[6]	ENET0_MDIO	I2C4_SDA		GPIO4_IO13
J3.26	GPT0_CAPTURE	I2C1_SDA	KPP0_COL5	GPIO0_IO15
J3.29	M40_GPIO0_IO01	M40_TPM0_CH1	UART4_TX	GPIO0_IO09
J3.30	GPT0_CLK	I2C1_SCL	KPP0_COL4	GPIO0_IO14
J3.31[2]	ENET1_RGMII_TXD3	UART3_RTS_B	TSI_S1_SYNC	GPIO6_IO15

Pin #	Alt 0	Alt 1	Alt 2	Alt 3
J3.32	M40_I2C0_SDA	M40_UART0_TX	M40_GPIO0_IO03	GPIO0_IO07
J3.33	USDHC1_DATA6	NAND_WE_B	USDHC1_WP	GPIO5_IO21
J3.34	M40_GPIO0_IO00	M40_TPM0_CH0	UART4_RX	GPIO0_IO08
J3.35	USDHC1_DATA5	NAND_RE_B		GPIO5_IO20
J3.36	M41_I2C0_SDA	M41_UART0_TX	M41_GPIO0_IO03	GPIO0_IO11
J3.37	USDHC1_CMD			GPIO5_IO14
J3.38	M40_I2C0_SCL	M40_UART0_RX	M40_GPIO0_IO02	GPIO0_IO06
J3.39	USDHC1_DATA4	NAND_CE0_B		GPIO5_IO19
J3.40	M41_GPIO0_IO00	M41_TPM0_CH0	UART3_RX	GPIO0_IO12
J3.41	USDHC1_DATA3	NAND_DQS_P		GPIO5_IO18
J3.42	USDHC1_STROBE	NAND_CE1_B		GPIO5_IO23
J3.43	USDHC1_DATA2	NAND_DQS_N		GPIO5_IO17
J3.44	USDHC1_DATA7	NAND_ALE	USDHC1_CD_B	GPIO5_IO22
J3.45	USDHC1_DATA1	NAND_RE_P		GPIO5_IO16
J3.47	USDHC1_DATA0	NAND_RE_N		GPIO5_IO15
J4.5	HSIO_PCIE1_CLKREQ_B			GPIO4_IO30
J4.7	HSIO_PCIE0_WAKE_B			GPIO4_IO28
J4.9	HSIO_PCIE1_WAKE_B			GPIO4_IO31
J4.11	HSIO_PCIE0_CLKREQ_B			GPIO4_IO27
J4.13	HSIO_PCIE0_PERST_B			GPIO4_IO29
J4.15	HSIO_PCIE1_PERST_B			GPIO5_IO00
J4.21[5]	USB_HSIC0_STROBE	I2C1_SCL		GPIO5_IO02
J4.23[5]	USB_HSIC0_DATA	I2C1_SDA		GPIO5_IO01
J4.27	ESAI1_TX4_RX1			GPIO2_IO12
J4.31	SAI1_RXFS	SAI0_RXD		GPIO3_IO14
J4.32	SPDIF0_TX	MQS_L	ACM_MCLK_OUT1	GPIO2_IO15
J4.34	SPI3_CS1			GPIO2_IO21
J4.35	USDHC1_RESET_B			GPIO4_IO07
J4.36	SPDIF0_RX	MQS_R	ACM_MCLK_IN1	GPIO2_IO14
J4.37	ESAI1_TX1	SAI2_RXFS		GPIO2_IO09
J4.38	SPDIF0_EXT_CLK	DMA0_REQ_IN0		GPIO2_IO16
J4.40	SPI3_SDI	FTM_CH1		GPIO2_IO19
J4.42	SPI2_SDI			GPIO3_IO09
J4.43	ESAI1_TX2_RX3			GPIO2_IO10
J4.44	SAI1_TXD	SAI1_RXC		GPIO3_IO16
J4.45	ESAI1_TX3_RX2			GPIO2_IO11
J4.46	ESAI1_SCKT	SAI2_RXC		GPIO2_IO07
J4.47	MLB_CLK[7]	SAI3_RXFS		GPIO3_IO27
J4.51	ENET1_REFCLK_125M_25M	ENET1_PPS		GPIO4_IO16

Pin #	Alt 0	Alt 1	Alt 2	Alt 3
J4.53	ENET0_REFCLK_125M_25M	ENET0_PPS		GPIO4_IO15
J4.55	I2C1_SDA	USB_OTG2_OC		GPIO4_IO06
J4.56	ESAI1_TX5_RX0			GPIO2_IO13
J4.57	I2C1_SDA	USB_OTG1_OC		GPIO4_IO05
J4.58	ADC_IN1		KPP0_COL1	GPIO3_IO19
J4.59	FLEXCAN2_RX			GPIO4_IO01
J4.60	ADC_IN0		KPP0_COL0	GPIO3_IO18
J4.61	FLEXCAN2_TX			GPIO4_IO02
J4.62	ADC_IN6	SPI1_CS0	KPP0_ROW2	GPIO3_IO24
J4.63	I2C1_SCL	USB_OTG2_PWR		GPIO4_IO04
J4.64	ADC_IN4	SPI1_SDO	KPP0_ROW0	GPIO3_IO22
J4.65	I2C1_SCL	USB_OTG1_PWR		GPIO4_IO03
J4.66	ADC_IN5	SPI1_SDI	KPP0_ROW1	GPIO3_IO23
J4.67	SAI1_TXC	SAI0_TXC		GPIO3_IO15
J4.68	ADC_IN3	SPI1_SCK	KPP0_COL3	GPIO3_IO21
J4.69	SAI1_RXC	SAI0_TXD		GPIO3_IO12
J4.70	ADC_IN7	SPI1_CS1	KPP0_ROW3	GPIO3_IO25
J4.71	SPI2_SCK			GPIO3_IO07
J4.72	ADC_IN2		KPP0_COL2	GPIO3_IO20
J4.73[3]	ENET1_MDC	I2C4_SCL		GPIO4_IO18
J4.74	FLEXCAN1_RX			GPIO3_IO31
J4.75[3]	ENET1_MDIO	I2C4_SDA		GPIO4_IO17
J4.76	FLEXCAN1_TX			GPIO4_IO00
J4.79	FLEXCAN0_RX			GPIO3_IO29
J4.80	FLEXCAN0_TX			GPIO3_IO30
J4.82	MLB_DATA[7]	SAI3_RXD		GPIO3_IO28
J4.84	MLB_SIG[7]	SAI3_RXC		GPIO3_IO26

Note [1]: Signals are shared with the On-SOM Bluetooth.
Note [2]: There is an assembly option to expose RGMII interface.
Note [3]: I2C4 interface is used by CODEC on the SOM
Pin configuration for I2C4 signal can't be changed.
Note [4]: DSI0 interface is not accessible when LVDS option is assembled.
Note [6]: The pin mode cannot be changed on SOMs that have at least one Ethernet PHY assembled.
Note [7]: MLB Interface was removed. Do not use.

8 SOM's Interfaces

Trace Impedance

SOM traces are designed with the below table impedance list per signal group.
Table is a reference when you are updating or creating constraints in the PCB design tool to set up the impedances/trace widths.

Table 8: SOM Signal Group Traces Impedance

Signal Group	Impedance
All single ended signals	50 Ω Single ended
PCIe TX/RX data pairs	85 Ω Differential
USB Differential signals	90 Ω Differential
Differential signals including: Ethernet, PCIe clocks, HDMI, MIPI (CSI and DSI), LVDS lines	100 Ω Differential

8.1 Display Interfaces

- HDMI/DP/eDP
  - HDMI1.4, HDMI 2.0a support for resolution up to 4096x2160p60
  - HDCP 2.2 and HDCP 1.4
  - Pixel clock up to 596 MHz
  - Display Port 1.3
  - eDP 1.4
  - One standard support at a time by means of software configuration.
  - All standards share the same pins.
- MIPI DSI
  - Bidirectional communication
  - Programmable display resolutions
  - Multiple peripheral support capability, configurable virtual channels
  - Video mode pixel formats, 16 bpp (5,6,5 RGB),
  - 18 bpp (6,6,6 RGB) packed, 18 bpp (6,6,6 RGB) loosely, 24 bpp (8,8,8 RGB)
- LVDS
  - Resolution up to 1920x1080.
  - Each LVDS link has 4 data lanes + 1 CLK lane.

8.1.1 HDMI

Table 9: HDMI Signals

Pin #	Pin name	Ball
J2.51	HDMI_TX0_AUX_M	BG3
J2.49	HDMI_TX0_AUX_P	BH2
J2.61	HDMI_TX0_CEC	BJ1
J2.67	HDMI_TX0_DDC_SCL	BG1
J2.65	HDMI_TX0_DDC_SDA	BN5
J2.63	HDMI_TX0_HPD	BH8
J2.88	HDMI_TX0_I2C0_SCL	BN9
J2.90	HDMI_TX0_I2C0_SDA	BN7
J2.39	HDMI_TX0_TX_M_LN_0	BM8
J2.43	HDMI_TX0_TX_M_LN_1	BM6
J2.47	HDMI_TX0_TX_M_LN_2	BM4
J2.57	HDMI_TX0_TX_M_LN_3	BK2
J2.37	HDMI_TX0_TX_P_LN_0	BL9
J2.41	HDMI_TX0_TX_P_LN_1	BL7
J2.45	HDMI_TX0_TX_P_LN_2	BL5
J2.55	HDMI_TX0_TX_P_LN_3	BL3

8.1.1.1 HDMI Termination

HDMI CLK and Data lines (TMDS type) should be terminated using 604-Ohm resistors. Termination should be applied after HDMI analog core is powered. SPEAR-MX8 power SW_1P8 pins can be used for the termination control. See Figure 3 for illustration of the termination scheme.

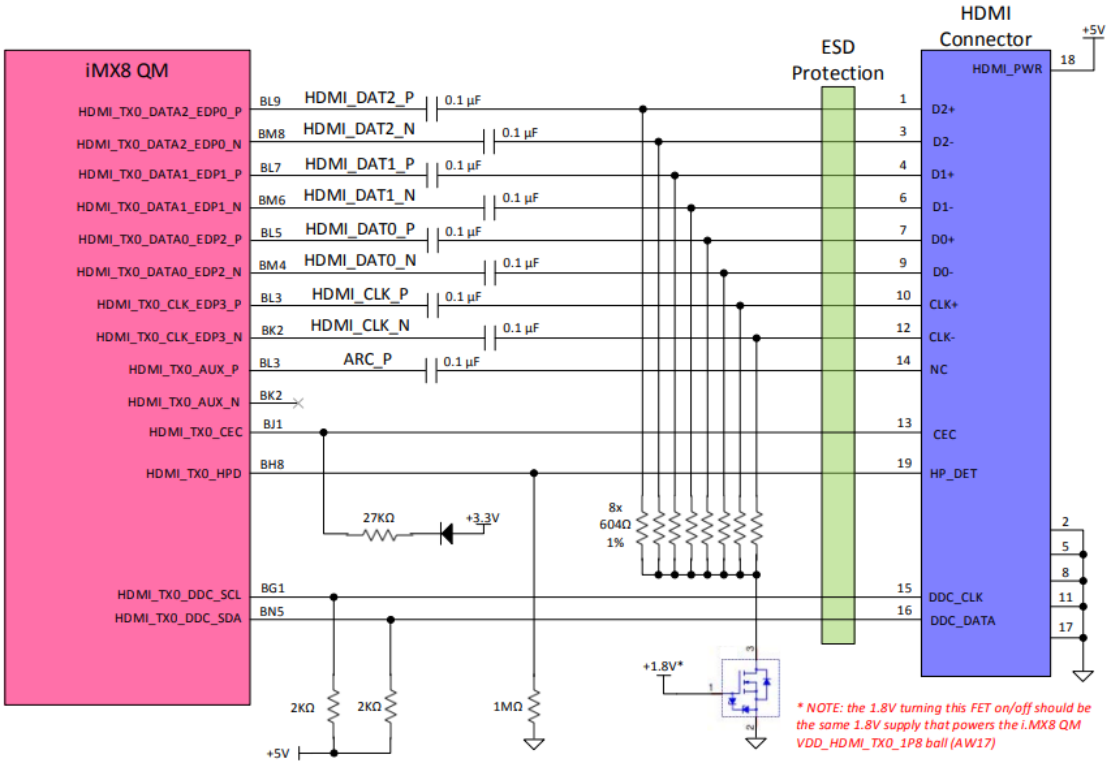


Figure 3 : HDMI output connectivity

When planning the HDMI interface, place the 604 Ω pull-down resistors directly on the signal trace, as shown in Figure 4.

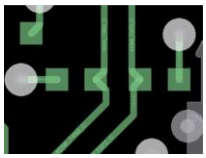


Figure 4: HDMI interface pull-down resistor placement

8.1.2 Display Port/Embedded Display Port

The Display port and Embedded Display port signals share the same pins as the HDMI interface with appropriate software changes to output the different display standard.

DisplayPort 1.3 standard (VESA.org)

- DP supports 1.6 GHz (RBR), 2.7 GHz (HBR), and 5.4 GHz (HBR2) rates. Those rates are managed in API (Host).
- RBR supports 1080p60 (RGB 8b), HBR supports 4kp30 (RGB 8b) and HBR2 supports 4kp60 (RGB 8b).

Embedded DisplayPort 1.4 standard (VESA.org)

- eDP link rates: R216 (2.16 Gbps), R243 (2.43 Gbps), R324 (3.24 Gbps), and R432 (4.32 Gbps)
- Fast Link Training is also supported

Table 10: Display Port/ Embedded DP Signals

Pin #	Pin name	Ball
J2.51	EDP_AUX_N	BG3
J2.49	EDP_AUX_P	BH2
J2.39	EDP0_N	BM8
J2.43	EDP1_N	BM6
J2.47	EDP2_N	BM4
J2.57	EDP3_N	BK2
J2.37	EDP0_P	BL9
J2.41	EDP1_P	BL7
J2.45	EDP2_P	BL5
J2.55	EDP3_P	BL3

8.1.2.1 DP/eDP Termination

DP/eDP CLK and Data lines should be bypassed using 0.1µF Capacitors.

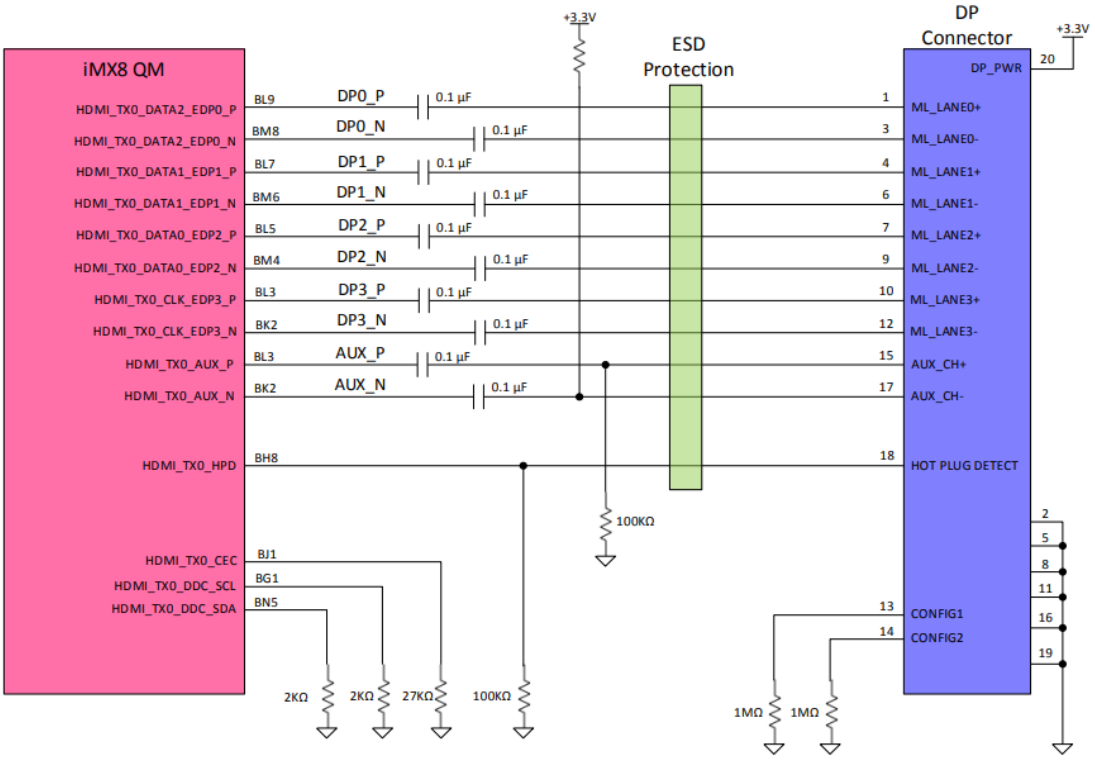


Figure 5 : DP/eDP output connectivity

8.1.3 MIPI-DSI

Table 11: MIPI-DSI Signals

Pin #	Pin name	Ball
J1.20[4]	MIPI_DSI0_CLK_N	BN27
J1.22[4]	MIPI_DSI0_CLK_P	BL27
J1.28[4]	MIPI_DSI0_DATA0_N	BM28
J1.26[4]	MIPI_DSI0_DATA0_P	BK28
J1.32[4]	MIPI_DSI0_DATA1_N	BM26
J1.30[4]	MIPI_DSI0_DATA1_P	BK26
J1.36[4]	MIPI_DSI0_DATA2_N	BN29
J1.34[4]	MIPI_DSI0_DATA2_P	BL29
J1.40[4]	MIPI_DSI0_DATA3_N	BN25
J1.38[4]	MIPI_DSI0_DATA3_P	BL25
J1.76[4]	MIPI_DSI0_GPIO0_00	BD28
J1.78[4]	MIPI_DSI0_GPIO0_01	BD30
J1.70[4]	MIPI_DSI0_I2C0_SCL	BE29
J1.68[4]	MIPI_DSI0_I2C0_SDA	BE31

Note [4]: DSI0 interface is not accessible when LVDS option is assembled.

8.1.4 LVDS Display

The SOM uses two channel LVDS Display ports.
These outputs are used to communicate RGB data and controls to external LCD displays.

Table 12: LVDS Display Channel 0 Signals

Pin #	Pin name	Ball
J1.89	LVDS0_GPIO0_IO00	BE39
J1.90	LVDS0_GPIO0_IO01	BD40
J1.86	LVDS0_I2C0_SCL	BD38
J1.84	LVDS0_I2C0_SDA	BD36
J1.82	LVDS0_I2C1_SCL	BE37
J1.80	LVDS0_I2C1_SDA	BE35
J1.55	LVDS0_T0AN	BK42
J1.53	LVDS0_T0AP	BM42
J1.51	LVDS0_T0BN	BL43
J1.49	LVDS0_T0BP	BN43
J1.61	LVDS0_T0CLKN	BL41
J1.59	LVDS0_T0CLKP	BN41
J1.47	LVDS0_T0CN	BK44
J1.45	LVDS0_T0CP	BM44
J1.43	LVDS0_T0DN	BL45
J1.41	LVDS0_T0DP	BN45
J1.79	LVDS0_T1AN	BG43
J1.77	LVDS0_T1AP	BH44
J1.75	LVDS0_T1BN	BG41
J1.73	LVDS0_T1BP	BH42
J1.85	LVDS0_T1CLKN	BG45
J1.83	LVDS0_T1CLKP	BH46
J1.71	LVDS0_T1CN	BG39
J1.69	LVDS0_T1CP	BH40
J1.67	LVDS0_T1DN	BG37
J1.65	LVDS0_T1DP	BH38

Table 13: LVDS Display Channel 1 Signals

Pin #	Pin name	Ball
J1.74	LVDS1_I2C0_SCL	BL35
J1.72	LVDS1_I2C0_SDA	BE33
J1.52	LVDS1_T0AN	BL37
J1.50	LVDS1_T0AP	BN37
J1.56	LVDS1_T0BN	BK38
J1.54	LVDS1_T0BP	BM38
J1.46	LVDS1_T0CLKN	BK36
J1.44	LVDS1_T0CLKP	BM36
J1.60	LVDS1_T0CN	BL39
J1.58	LVDS1_T0CP	BN39
J1.64	LVDS1_T0DN	BK40
J1.62	LVDS1_T0DP	BM40

Note: There is an assembly option to upgrade second LVDS to dual channel. Please contact sales@variscite.com for more information

8.2 HDMI RX

Due to NXP PCN 202012002I the HDMI RX Interface was removed.

Table 14: Removed HDMI RX Signals

Pin #	Pin name	Ball
J2.15	NC (Removed HDMI_RX0_ARC_M)	BL13
J2.13	NC (Removed HDMI_RX0_ARC_P)	BM14
J2.25	NC (Removed HDMI_RX0_CEC)	BJ9
J2.31	NC (Removed HDMI_RX0_DDC_SCL)	BH10
J2.29	NC (Removed HDMI_RX0_DDC_SDA)	BE13
J2.27	NC (Removed HDMI_RX0_HPD)	BF14
J2.33	NC (Removed HDMI_RX0_MON_5V)	BN11
J2.21	NC (Removed HDMI_RX0_RX_CLK_M)	BL11
J2.19	NC (Removed HDMI_RX0_RX_CLK_P)	BM12
J2.11	NC (Removed HDMI_RX0_RX_M_LN_0)	BL15
J2.7	NC (Removed HDMI_RX0_RX_M_LN_1)	BL17
J2.3	NC (Removed HDMI_RX0_RX_M_LN_2)	BL19
J2.9	NC (Removed HDMI_RX0_RX_P_LN_0)	BM16
J2.5	NC (Removed HDMI_RX0_RX_P_LN_1)	BM18
J2.1	NC (Removed HDMI_RX0_RX_P_LN_2)	BM20

8.3 Camera Interface

The SOM consist of two CSI-2 Host Controllers which implements all protocol functions defined in the MIPI CSI-2 specification, providing an interface between the SOM and the MIPI D-PHY, allowing communication with an MIPI CSI-2 compliant camera sensor.

The MIPI CSI-2 host controller supports the following features:

- Compliance with MIPI Alliance standard for camera serial interface 2 (CSI-2), version 1.00 29th November, 2005
- Optional support for Camera Control Interface (CCI) using DesignWare Core (DW_apb_i2c)
- Interface with MIPI D-PHY following PHY Protocol Interface (PPI), as defined in MIPI Alliance Specification for D-PHY, version 1.00.00 14th May, 2009
- Up to 4 D-PHY Rx data lanes
- Dynamically configurable multi-lane merging
- Long and short packet decoding
- Timing accurate signaling of frame and line synchronization packets
- Support for several frame formats such as:
    - General frame or digital interlaced video with or without accurate sync timing
    - Data type (packet or frame level) and virtual channel interleaving
- 32-bit image data interface delivering data formatted as recommended in CSI-2 specification
- Supports all primary and secondary data formats:
    - RGB, YUV and RAW color space definitions
    - From 24-bit down to 6-bit per pixel
    - Generic or user-defined byte-based data types
- Error detection and correction:

Table 15: MIPI-CSI2 Port 0 Signals

Pin #	Pin name	Ball
J2.2	MIPI_CSI0_ACM_MCLK_OUT	BJ23
J2.50	MIPI_CSI0_CKN	BE21
J2.48	MIPI_CSI0_CKP	BF20
J2.56	MIPI_CSI0_DN0	BE23
J2.60	MIPI_CSI0_DN1	BE19
J2.64	MIPI_CSI0_DN2	BE25
J2.68	MIPI_CSI0_DN3	BE17
J2.54	MIPI_CSI0_DP0	BF22
J2.58	MIPI_CSI0_DP1	BF18
J2.62	MIPI_CSI0_DP2	BF24
J2.66	MIPI_CSI0_DP3	BF16
J2.10	MIPI_CSI0_GPIO0_IO00	BL23
J2.12	MIPI_CSI0_GPIO0_IO01	BM22
J2.6	MIPI_CSI0_I2C0_SCL	BH24
J2.14	MIPI_CSI0_I2C0_SDA	BN19

Table 16: MIPI-CSI2 Port 1 Signals

Pin #	Pin name	Ball
J2.4	MIPI_CSI1_ACM_MCLK_OUT	BN23
J2.26	MIPI_CSI1_CKN	BH16
J2.24	MIPI_CSI1_CKP	BJ17
J2.32	MIPI_CSI1_DN0	BH18
J2.36	MIPI_CSI1_DN1	BH14
J2.40	MIPI_CSI1_DN2	BH20
J2.44	MIPI_CSI1_DN3	BH12
J2.30	MIPI_CSI1_DP0	BJ19
J2.34	MIPI_CSI1_DP1	BJ15
J2.38	MIPI_CSI1_DP2	BJ21
J2.42	MIPI_CSI1_DP3	BJ13
J2.18	MIPI_CSI1_GPIO0_IO00	BN15
J2.20	MIPI_CSI1_GPIO0_IO01	BN13
J2.16	MIPI_CSI1_I2C0_SCL	BN17
J2.8	MIPI_CSI1_I2C0_SDA	BE15

8.4 Ethernet Interface

The SOM consists of dual Ethernet Media Access Controller (MAC) designed to support 10/100/1000 Mbps Ethernet/IEEE 802.3 networks. The Following External Gigabit magnetics are required to complete the interface to the media. The i.MX8 processor also consists of HW assist for IEEE1588 standard. See the IEEE1588 section for more details.

The On SOM Atheros AR8033 / ADIN1300 Gigabit PHY in conjunction with external magnetics on carrier board complete the interface to the media.

Table 17: Gigabit Ethernet Magnetics

Vendor	P/N	Package	Cores	Configuration
Pulse	H5007NL	Transformer	8	Auto-MDX
TDK	TLA-7T101LF	Transformer	8	Auto-MDX
Pulse	J0G-0009NL	Integrated RJ45	8	Auto-MDX

Table 18: Ethernet PHY Port 0 Signals

Pin #	Pin name	Ball
J3.17	ETH0_LED_ACT	AR8033.23/ ADIN1300.21 (via inv. FET)
J3.21	ETH0_LED_LINK_10_100	AR8033.26/ ADIN1300-GND
J3.19	ETH0_LED_LINK_1000	AR8033.24/ ADIN1300.26 (via level shifter)
J3.3	ETH0_MDI_A_M	AR8033.12/ ADIN1300.13
J3.1	ETH0_MDI_A_P	AR8033.11/ ADIN1300.12
J3.7	ETH0_MDI_B_M	AR8033.15/ ADIN1300.15
J3.5	ETH0_MDI_B_P	AR8033.14/ ADIN1300.14
J3.11	ETH0_MDI_C_M	AR8033.18/ ADIN1300.17
J3.9	ETH0_MDI_C_P	AR8033.17/ ADIN1300.16
J3.15	ETH0_MDI_D_M	AR8033.21/ ADIN1300.19
J3.13	ETH0_MDI_D_P	AR8033.20/ ADIN1300.18

Table 19: Ethernet PHY Port 1 Signals

Pin #	Pin name	Ball
J3.18[2]	ETH1_LED_ACT(ENET1_RGMII_TX_CTL)	AR8033.23/ ADIN1300.21 (via inv. FET) (B48)
J3.22[2]	ETH1_LED_LINK_10_100(ENET1_RGMII_TXC)	AR8033.26/ ADIN1300-GND (D46)
J3.20[2]	ETH1_LED_LINK_1000(ENET1_RGMII_TXD2)	AR8033.24/ ADIN1300.26 (via level shifter) (G47)
J3.4[2]	ETH1_MDI_A_M(ENET1_RGMII_RXD2)	AR8033.12/ ADIN1300.13 (D52)
J3.2[2]	ETH1_MDI_A_P(ENET1_RGMII_TXD0)	AR8033.11/ ADIN1300.12 (A49)
J3.8[2]	ETH1_MDI_B_M(ENET1_RGMII_TXD1)	AR8033.15/ ADIN1300.15 (C47)
J3.6[2]	ETH1_MDI_B_P(ENET1_RGMII_RXD3)	AR8033.14/ ADIN1300.14 (E53)
J3.12[2]	ETH1_MDI_C_M(ENET1_RGMII_RX_CTL)	AR8033.18/ ADIN1300.17 (E49)
J3.10[2]	ETH1_MDI_C_P(ENET1_RGMII_RXC)	AR8033.17/ ADIN1300.16 (B50)
J3.16[2]	ETH1_MDI_D_M(ENET1_RGMII_RXD1)	AR8033.21/ ADIN1300.19 (C51)
J3.14[2]	ETH1_MDI_D_P(ENET1_RGMII_RXD0)	AR8033.20/ ADIN1300.18 (E51)

Note [2]: There is an assembly option to expose RGMII interface.
Voltage Level of these pins on SOM PCB Revisions up to 1.3 is 3.3V.
ON PCB Revisions 1.3 and up, RGMII Interface can be 3.3V (By default) or 1.8V.
The selection is done using GPIO2_IO27.
Low level of this GPIO will select 3.3V, high level will select 1.8V.
Please contact sales@variscite.com for more information

Table 20: AR8033 Ethernet PHY LED Behavior

Symbol	10M link	10M active	100M link	100M active	1000M link	1000M active
LED_LINK_10_100	OFF	OFF	ON	ON	OFF	OFF
LED_LINK_1000	OFF	OFF	OFF	OFF	ON	ON
LED_ACT	ON	BLINK	ON	BLINK	ON	BLINK
ON = active; OFF = inactive						

Table 21: ADIN1300 Ethernet PHY LED Behavior

Symbol	10M link	10M active	100M link	100M active	1000M link	1000M active
LED_LINK_10_100	OFF	OFF	OFF	OFF	OFF	OFF
LED_LINK_1000	ON	ON	ON	ON	ON	ON
LED_ACT	ON	BLINK	ON	BLINK	ON	BLINK
ON = active; OFF = inactive						

Table 22: MDIO Signals

Pin #	Pin name	Ball
J3.23[6]	ENET0_MDC	A9
J3.24[6]	ENET0_MDIO	D10

Note [6]: The pin mode cannot be changed on SOMs that have at least one Ethernet PHY assembled.

8.5 Secure Digital Host Controller

The SOM features an MMC/SD/SDIO interface:

- Fully compliant with MMC command/response sets and physical layer as defined in the Multimedia Card System specification v4.2/4.3/4.4, including high-capacity (size > 2 GB) cards HC MMC.
- Fully compliant with SD command/response sets and physical layer as defined in the SD Memory Card specifications v3.0, including high-capacity SDHC
- Fully compliant with SDIO command/response sets and interrupt/read-wait mode as defined in the SDIO Card specification, Part E1 v1.10
- Fully compliant with SD Card specification, Part A2, SD Host Controller Standard specification v2.00
- 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR104 mode (104 MB/s max)
- 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 52 MHz in both SDR and DDR modes (104 MB/s max). However, the SoC level integration and I/O mixing logic restrict functionality to the following:
    -

Table 23: SDMMC1 Signals

Pin #	Pin name	Ball
J3.49	USDHC1_CLK	J39
J3.37	USDHC1_CMD	G41
J3.47	USDHC1_DATA0	E37
J3.45	USDHC1_DATA1	F38
J3.43	USDHC1_DATA2	E39
J3.41	USDHC1_DATA3	F40
J3.39	USDHC1_DATA4	H40
J3.35	USDHC1_DATA5	G43
J3.33	USDHC1_DATA6	F42
J3.44	USDHC1_DATA7	H42
J4.35	USDHC1_RESET_B	A5
J3.42	USDHC1_STROBE	J43

8.6 USB 2.0

The SOM consists of a three USB controller blocks which provides a high performance USB functionality that conforms to the USB 2.0 specification.

Table 24: USB 2.0 Channel 1 Signals

Pin #	Pin name	Ball
J3.48	USB_OTG1_DN	C39
J3.46	USB_OTG1_DP	B40
J3.55	USB_OTG1_ID	A37
J3.53	USB_OTG1_VBUS	A39

Table 25: USB 2.0 Channel 2 Signals

Pin #	Pin name	Ball
J3.54	USB_OTG2_DM	C37
J3.52	USB_OTG2_DP	B38
J3.25	USB_OTG2_ID	F30
J3.57	USB_OTG2_VBUS	A35

Table 26: HSIC USB 2.0 Signals

Pin #	Pin name	Ball
J4.23[5]	USB_HSIC0_DATA	H26
J4.21[5]	USB_HSIC0_STROBE	F28
J4.19[5]	VCC_HSIC	V26

Note [5]: VCC_HSIC should be 1.2V if HSIC interface is in use.

8.7 USB 3.0

The SOM includes a Super-speed USB 3.0 core consisting of:

- HS/FS/LS UTMI compliant interface
- High speed, full speed and low speed operation in host mode (with UTMI transceiver)
- High speed, and full speed operation in peripheral mode (with UTMI transceiver)
- Hardware support for OTG signaling, session request protocol, and host negotiation protocol
- Up to 8 bidirectional endpoints
- Integrated HS USB PHY

Table 27: USB3 Signals

Pin #	Pin name	Ball
J3.60	USB_SS3_RX_M_LN_0	B34
J3.58	USB_SS3_RX_P_LN_0	C35
J3.66	USB_SS3_TX_M_LN_0	B32
J3.64	USB_SS3_TX_P_LN_0	A33

8.8 Audio

The SOM features three audio interfaces

- WM8904CGEFL Audio codec interfaces:
  - Analog outputs & inputs: stereo line-in & Stereo HP out.
  - Digital microphone input
- Enhanced Serial Audio Interface
- Serial Audio Interface
- S/PDIF in/out

Analog audio signals are part of the SOM WM8904 audio codec, available with **"AC" Configuration** only.

The Codec features stereo ground-referenced headphone amplifiers using the Wolfson 'Class-W' amplifier techniques -incorporating an innovative dual-mode charge pump architecture - to optimize efficiency and power consumption during playback. The ground-referenced headphone and line outputs eliminate AC coupling capacitors, and both outputs include common mode feedback paths to reject ground noise.

The following figure illustrates the connectivity for no large AC coupling capacitors

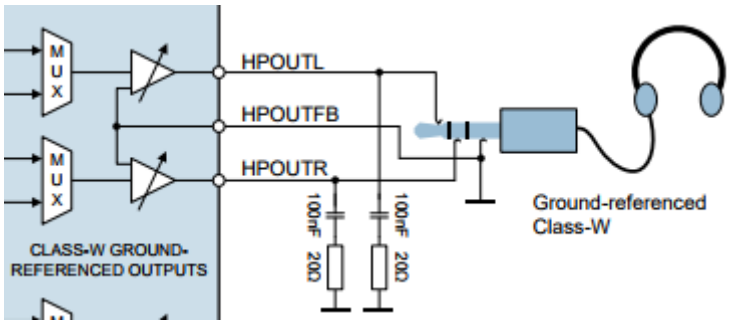


Figure 6: WM8904 Headphone connectivity

8.8.1 WM8904CGEFL Audio Codec

Table 28: Analog audio Signals

Pin #	Pin name	Ball
J4.81	DMIC_CLK	WM8904CGEFL.1
J4.83	DMIC_DATA	WM8904CGEFL.27
J4.85	HPLOUT	WM8904CGEFL.13
J4.86	LINEIN1_RP	WM8904CGEFL.24
J4.87	HPROUT	WM8904CGEFL.15
J4.88	LINEIN1_LP	WM8904CGEFL.26
J4.89	HPOUTFB	WM8904CGEFL.14
J4.90	AGND	WM8904CGEFL.22

8.8.2 Enhanced Serial Audio Interface

The Enhanced Serial Audio Interface (ESAI) provides a full-duplex serial port for serial communication with a variety of serial devices, including industry-standard codecs, SPDIF transceivers, and other processors. The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. All serial transfers are synchronized to a clock. Additional synchronization signals are used to delineate the word frames. The normal mode of operation is used to transfer data at a periodic rate, one word per period. The network mode is also intended for periodic transfers; however, it supports up to 32 words (time slots) per period. This mode can be used to build time division multiplexed (TDM) networks. In contrast, the on-demand mode is intended for non-periodic transfers of data and to transfer data serially at high speed when the data becomes available.

Table 29: Enhanced Serial Audio Interface 1 Signals

Pin #	Pin name	Ball
J2.79	ESAI1_TX0	BF10
J2.81	ESAI1_FSR	BE11
J2.83	ESAI1_SCKR	BD12
J2.85	ESAI1_FST	BF12
J4.27	ESAI1_TX4_RX1	AY12
J4.37	ESAI1_TX1	BA11
J4.43	ESAI1_TX2_RX3	AU11
J4.45	ESAI1_TX3_RX2	AV10
J4.46	ESAI1_SCKT	AY10
J4.56	ESAI1_TX5_RX0	AT10

8.8.3 Serial Audio Interface

SAI module provides a synchronous audio interface that supports full duplex serial interfaces with frame synchronization, such as I2S, AC97, TDM, and codec/DSP interfaces.

Table 30: Serial Audio Interface 0 Signals

Pin #	Pin name	Ball
J2.74	SAI0_RXC	BB4
J2.72	SAI0_RXD	BA5
J2.78	SAI0_RXFS	BC1
J2.80	SAI0_TXC	BA3
J2.76	SAI0_TXD	AY6
J2.89	SAI0_TXFS	AY2

Table 31: Serial Audio Interface 1 Signals

Pin #	Pin name	Ball
J4.69	SAI1_RXC	AV6
J2.71	SAI1_RXD	AV4
J4.31	SAI1_RXFS	AU3
J4.67	SAI1_TXC	AU5
J4.44	SAI1_TXD	AU1
J2.73	SAI1_TXFS	AV2

Table 32: Serial Audio Interface 2 Signals

Pin #	Pin name	Ball
J4.46	SAI2_RXC	AY10
J2.79	SAI2_RXD	BF10
J4.37	SAI2_RXFS	BA11

Table 33: Serial Audio Interface 3 Signals

Pin #	Pin name	Ball
J4.84	SAI3_RXC	E1
J4.82	SAI3_RXD	E3
J4.47	SAI3_RXFS	D2

8.8.4 Sony Phillips Digital Interface In/Out

Sony/Philips Digital Interface (SPDIF) audio block is a stereo transceiver that allows the processor to receive and transmit digital audio. The SPDIF transceiver allows the handling of both SPDIF channel status (CS) and User (U) data and includes a frequency measurement block that allows the precise measurement of an incoming sampling frequency.

Table 34: S/PDIF Signals

Pin #	Pin name	Ball
J4.32	SPDIF0_TX	BC9
J4.36	SPDIF0_RX	BC7
J4.38	SPDIF0_EXT_CLK	BD6

8.9 PCIe

The PCIe IP provides PCI Express Gen 3.0 functionality.
The following list the key features of the PCIe PHY:

- 1.5 / 2.5 / 3.0 / 5.0 / 6.0 Gbps Serializer / Deserializer
- Compliant with PCI Express Base Specification 2.1
- Compliant with PIPE Specification 2.0
- 8 / 16 / 20 / 40-bit CMOS Interface for Transmitter and Receiver
- 25 / 100 MHz Reference Clock
- K28.5 Detection for Word Alignment
- 8B/10B Encoding / Decoding
- Receiver Detection
- 28 nm CMOS Process (LN28LPP)
- Supports Spread Spectrum Clocking in Transmitter and Receiver

Table 35: PCIE Common Clock Signals

Pin #	Pin name	Ball
J4.2	HSIO_PCIE_IOB_EXT_REFCLK100M_N	E25
J4.4	HSIO_PCIE_IOB_EXT_REFCLK100M_P	F26

Note: Clock signals acts as output from the SOM for Gen1 and Gen2 operation.
Clock acts as input for Gen3 operation.

Table 36: PCIE0 Signals

Pin #	Pin name	Ball
J4.11	HSIO_PCIE0_CLKREQ_B	A17
J4.13	HSIO_PCIE0_PERST_B	D20
J4.10	HSIO_PCIE0_RX0_N	B30
J4.8	HSIO_PCIE0_RX0_P	A29
J4.16	HSIO_PCIE0_TX0_N	C27
J4.14	HSIO_PCIE0_TX0_P	B26
J4.7	HSIO_PCIE0_WAKE_B	A15

Table 37: PCIE2 Signals

Pin #	Pin name	Ball
J4.22	HSIO_PCIE2_RX0_N	B20
J4.20	HSIO_PCIE2_RX0_P	A19
J4.28	HSIO_PCIE2_TX0_N	C17
J4.26	HSIO_PCIE2_TX0_P	B16

8.10 Serial ATA

The SOM consists of an integrated Serial Advanced Technology Attachment (SATA) controller that is compatible with the Advanced Host Controller Interface (AHCI) specification. The SATA

Controller block (SATA), along with integrated physical link hardware (SATA PHY), provides one SATA port for the attachment of external SATA compliant storage devices.

Table 38: SATA Signals

Pin #	Pin name	Ball
J4.22	SATA_RX_N	B20
J4.20	SATA_RX_P	A19
J4.28	SATA_TX_N	C17
J4.26	SATA_TX_P	B16

8.11 UART

- High-speed TIA/EIA-232-F compatible, up to 5.0 Mbit/s
- Serial IR interface low-speed, IrDA-compatible (up to 115.2 Kbit/s)
- 9-bit or multi drop mode (RS-485) support (automatic slave address detection)
- 7, 8, 9, or 10-bit data characters (7-bits only with parity), 1 or 2 stop bits
- Programmable parity (even, odd, and no parity)
- Hardware flow control support for RTS and CTS signals

Table 39: UART0 Signals

Pin #	Pin name	Ball
J1.12	UART0_CTS_B	AW49
J1.14	UART0_RTS_B	AU45
J1.16	UART0_RX	AV50
J1.10	UART0_TX	AV48

Note: UART0 used as serial console of the main ARM cores.

Table 40: UART1 Signals

Pin #	Pin name	Ball
J1.4[1]	UART1_CTS_B	AV46
J1.6[1]	UART1_CTS_B	AR43
J1.6[1]	UART1_RTS_B	AR43
J1.4[1]	UART1_RTS_B	AV46
J1.8[1]	UART1_RX	AT44
J1.2[1]	UART1_TX	AY48

Note [1]: Signals are shared with the On-SOM Bluetooth.

Table 41: UART2 Signals

Pin #	Pin name	Ball
J1.80	UART2_RX	BE35

Pin #	Pin name	Ball
J1.14	UART2_RX	AU45
J1.82	UART2_TX	BE37
J1.12	UART2_TX	AW49

Table 42: UART3 Signals

Pin #	Pin name	Ball
J3.10[2]	UART3_CTS_B	AR8033.17(B50)
J3.31[2]	UART3_RTS_B	(D48)
J3.6[2]	UART3_RX	AR8033.14(E53)
J3.40	UART3_RX	AP44
J3.20[2]	UART3_TX	AR8033.26(G47)
J1.11	UART3_TX	AU47

Note [2]: Pins are shared with the On-SOM Ethernet PHY2.

Table 43: UART4 Signals

Pin #	Pin name	Ball
J2.18	UART4_RX	BN15
J3.34	UART4_RX	AR47
J2.20	UART4_TX	BN13
J3.29	UART4_TX	AU53

8.12 Flexible Controller Area Network

The Flexible Controller Area Network (FLEXCAN) module is a communication controller supporting CAN-FD (CAN Flexible Data Rate) and CAN2.0B specification.
Signal Description:

- CAN Rx: The receive pin from the CAN bus transceiver. Dominant state is represented by logic level '0'. Recessive state is represented by logic level '1'.
- CAN Tx: The transmit pin to the CAN bus transceiver. Dominant state is represented by logic level '0'. Recessive state is represented by logic level '1'.

Table 44: CAN0 Signals

Pin #	Pin name	Ball
J4.79	FLEXCAN0_RX	C5
J4.80	FLEXCAN0_TX	H6

Table 45: CAN1 Signals

Pin #	Pin name	Ball
J4.74	FLEXCAN1_RX	E5
J4.76	FLEXCAN1_TX	G7

Table 46: CAN2 Signals

Pin #	Pin name	Ball
J4.59	FLEXCAN2_RX	C3
J4.61	FLEXCAN2_TX	E7

8.13 SPI

- Flexible sequence engine to support various flash vendor devices.
- Support for FPGA interface
- Single, dual, quad, and octal mode of operation.
- DDR/DTR mode wherein the data is generated on every edge of the serial flash clock.
- Support for flash data strobe signal for data sampling in DDR and SDR mode.
- Two identical serial flash devices can be connected and accessed in parallel for data read operations, forming one (virtual) flash memory with doubled readout bandwidth.

Table 47: SPI0 Signals

Pin #	Pin name	Ball
J2.78	SPI0_CS0	BC1
J2.80	SPI0_CS1	BA3
J2.72	SPI0_SDI	BA5
J2.76	SPI0_SDO	AY6
J2.74	SPI0_SCK	BB4

Table 48: SPI1 Signals

Pin #	Pin name	Ball
J4.62	SPI1_CS0	AL9
J4.70	SPI1_CS1	AP6
J4.68	SPI1_SCK	AR9
J4.66	SPI1_SDI	AR7
J4.64	SPI1_SDO	AN9

Table 49: SPI2 Signals

Pin #	Pin name	Ball
J2.75	SPI2_CS0	AW1
J4.71	SPI2_SCK	AW5
J4.42	SPI2_SDI	AY4
J2.77	SPI2_SDO	BA1

Table 50: ECSPI3 Signals

Pin #	Pin name	Ball
J1.4[1]	SPI3_CS0	AV46
J4.34	SPI3_CS1	BD8
J2.86	SPI3_SCK	BF6
J1.2[1]	SPI3_SCK	AY48
J1.6[1]	SPI3_SDI	AR43
J1.8[1]	SPI3_SDO	AT44

Note [1]: Signals are shared with the On-SOM Bluetooth.

8.14 I2C

The SOM consists of 4 I2C Interface connectivity peripherals which provides serial interface for external devices. Data rates of up to 400 kbps are supported.
In addition, there are dedicated low-speed I2C non-DMA I2C busses for
MIPI-DSI, LVDS, HDMI-TX, MIPI-CSI.

Table 51: I2C0 Signals

Pin #	Pin name	Ball
J2.10	I2C0_SCL	BL23
J2.88	I2C0_SCL	BN9
J2.88	I2C0_SCL	BN9
J2.12	I2C0_SDA	BM22
J2.90	I2C0_SDA	BN7
J2.90	I2C0_SDA	BN7

Table 52: I2C1 Signals

Pin #	Pin name	Ball
J3.30	I2C1_SCL	AY52
J4.21	I2C1_SCL	F28
J4.63	I2C1_SCL	L9
J4.65	I2C1_SCL	J9
J3.26	I2C1_SDA	AV52
J4.23	I2C1_SDA	H26
J4.55	I2C1_SDA	H10
J4.57	I2C1_SDA	F8

Table 53: I2C2 Signals

Pin #	Pin name	Ball
J1.5	I2C2_SCL	BA53
J1.3	I2C2_SDA	AY50

Table 54: I2C4 Signals

Pin #	Pin name	Ball
J3.23[6]	I2C4_SCL	A9
J4.73[3]	I2C4_SCL	A13
J3.24[6]	I2C4_SDA	D10
J4.75[3]	I2C4_SDA	C13

Note [3]: I2C4 interface is used by CODEC on the SOM
Pin configuration for I2C4 signal can't be changed.
Note [6]: The pin mode cannot be changed on SOMs that have at least one Ethernet PHY assembled.

Table 55: LVDS0 I2C Signals

Pin #	Pin name	Ball
J1.86	LVDS0_I2C0_SCL	BD38
J1.84	LVDS0_I2C0_SDA	BD36
J1.82	LVDS0_I2C1_SCL	BE37
J1.80	LVDS0_I2C1_SDA	BE35

Table 56: LVDS1 I2C Signals

Pin #	Pin name	Ball
J1.74	LVDS1_I2C0_SCL	BL35
J1.72	LVDS1_I2C0_SDA	BE33
J1.70[4]	LVDS1_I2C1_SCL	BE29
J1.68[4]	LVDS1_I2C1_SDA	BE31

Note [4]: LVDS1 I2C1 interface is not accessible when DSI option is assembled.

Table 57: DSI0 I2C Signals

Pin #	Pin name	Ball
J1.70[4]	MIPI_DSI0_I2C0_SCL	BE29
J1.68[4]	MIPI_DSI0_I2C0_SDA	BE31

Note [4]: DSI0 I2C0 interface is not accessible when LVDS option is assembled.

Table 58: M40 and M41 I2C Signals

Pin #	Pin name	Ball
J3.38	M40_I2C0_SCL	AM44
J3.32	M40_I2C0_SDA	AU51
J1.9	M41_I2C0_SCL	AR45
J3.36	M41_I2C0_SDA	AU49

8.15 Analog to Digital Converter

ADC is a 1.8 V 12-bit ADC with 16 channels analog input MUX and level-shifters for low-voltage digital interface. ADC supports conversion up to five logic groups (ChA / ChB / ChC / ChD / SW). Each group can select one channel from 0 - 15 physical channels.

Table 59: Analog to Digital Converter Signals

Pin #	Pin name	Ball
J4.60	ADC_IN0	AP10
J4.58	ADC_IN1	AN11
J4.72	ADC_IN2	AP8
J4.68	ADC_IN3	AR9
J4.64	ADC_IN4	AN9
J4.66	ADC_IN5	AR7
J4.62	ADC_IN6	AL9
J4.70	ADC_IN7	AP6

8.16 General Purpose Timer

Each GPT is a 32-bit “free-running” or “set and forget” mode timer with programmable prescaler and compare and capture register. A timer counter value can be captured using an external event and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in “set and forget” mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock.

Table 60: General Purpose Timer Signals

Pin #	Pin name	Ball
J3.26	GPT0_CAPTURE	AV52
J3.30	GPT0_CLK	AY52
J1.1	GPT0_COMPARE	AW53
J1.3	GPT1_CAPTURE	AY50
J1.5	GPT1_CLK	BA53
J1.7	GPT1_COMPARE	BA51

8.17 MediaLB

Due to NXP PCN 202012002I the MLB Interface was removed.

Table 61: Removed MediaLB Signals

Pin #	Pin name	Ball
J4.47	Do not use (MLB_CLK)	D2
J4.82	Do not use (MLB_DATA)	E3
J4.84	Do not use (MLB_SIG)	E1

8.18 System Control Unit

- Power control, clocks, reset
- Boot ROMs
- PMIC interface
- Resource Domain Controller

Table 62: System Control Unit Signals

Pin #	Pin name	Ball
J1.15	SCU_DSC_BOOT_MODE2	BJ53
J1.17	SCU_DSC_BOOT_MODE3	BA43
J1.19	SCU_DSC_BOOT_MODE5	BK52
J1.25	SCU_GPIO0_IO00	AU43
J1.23	SCU_GPIO0_IO01	AV44
J1.27	SCU_GPIO0_IO05	AY44
J1.29	SCU_GPIO0_IO06	BG49
J3.63	SCU_WDOG0_WDOG_OUT	BB50

Note: For boot modes please see Boot Configuration section.

8.19 Secure Non-Volatile Storage

Secure Non-Volatile Storage, including Secure Real Time Clock, Security State Machine, Master Key Control, and Violation/Tamper Detection and reporting.

Table 63: Secure Non-Volatile Storage

Pin #	Pin name	Ball
J1.21	SNVS_ON_OFF_BUTTON	BE47
J3.61	SNVS_PMIC_ON_REQ	BL51
J1.35	SNVS_TAMPER_IN0	BE41
J1.37	SNVS_TAMPER_IN1	BE43
J1.31	SNVS_TAMPER_OUT0	BD46
J1.33	SNVS_TAMPER_OUT1	BD42

8.20 General Purpose LDO

SOM exposes two general purposes LDO from PMIC2.
Each is 1.5V to 5.0V, 400 mA; 3% accuracy with optional load switch mode.

Table 64: LDO Signals

Pin #	Pin name	Ball
J4.52	P2_LDO3	PF8100VAA0ES-2.25
J4.54	P2_LDO3	PF8100VAA0ES-2.25
J4.48	P2_LDO4	PF8100VAA0ES-2.28
J4.50	P2_LDO4	PF8100VAA0ES-2.28

Note: P2_LDO3 can be used if turned on once on boot time. The latest PF8200 Errata does not recommend toggling LDO3 in runtime.

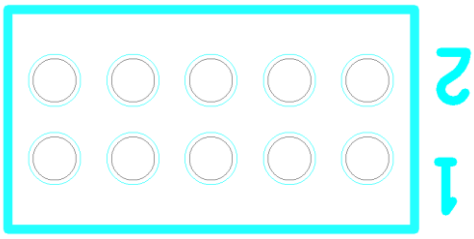
8.21 JTAG

The SOM consists of the System JTAG Controller (SJC) which provides debug and test control with maximum security. The test access port (TAP) is designed to support features compatible with the IEEE standard 1149.1 v2001 (JTAG). Support IEEE P1149.6 extensions to the JTAG standard are for AC testing of selected IO signals.

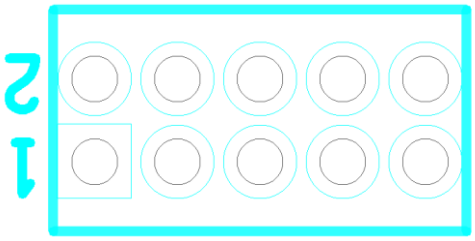
Table 65: JTAG signals 10-pin Header Connector

Pin #	Pin name	Ball
1	1.8V Reference voltage	
2	JTAG_TMS	BA49
3	GND	
4	JTAG_TCK	BC51
5	GND	
6	JTAG_TDO	BD52
7	4.7K Pull Down	
8	JTAG_TDI	BE51
9	JTAG_TRST_B	BE53
10	POR_B_1V8	BE49

Note: The connector footprint was changed on Rev 1.2 of the board.



SPEAR-MX8 Rev 1.1 and below



SPEAR-MX8 Rev 1.2 and up

8.22 Cortex M4

The SOM features two configurable Cortex-M4 subsystems and a dedicated Cortex-M4 subsystem within the SCU. The modular set of Cortex-M4 platform components offer a low-latency execution environment with real-time and low-power processing capability.
Along with the processor components, the Cortex-M4 subsystem features several off platform components. These off-platform components and subsystem features include:

- WDOG (watchdog) timer
- LPIT (Low-power Periodic Interrupt Timer) for periodic timer services
- TPM (Timer PWM Module) for timer and PWM services
    - 32-bit counters
- LPCG (Low-Power Clock Gating) for local clock management
- TSTMR (Timestamp Timer) for global timer services
    - Receives system time bus driven by system counter
- Power mode control
    - Programming model for power mode request
    - Low-power bus connected to SC to support power mode transitions
- Reset control and status
- MU (Messaging Unit) for inter-processor communication
    - MU0 with 4 channels inside the GP CM4 domain
    - MU1 with 1 channel which is inside the DSC. The latter is talked to over an asynchronous bus.
- LPI2C (Low-Power I2C) for serial communication
    - Standard features (FEATURE_EN = 1)
    - Slave mode logic enabled (SLAVE_EN = 1)
    - TX FIFO size of 4 entries (TXFIFO_SZ = 2)
    - RX FIFO size of 4 entries (RXFIFO_SZ = 2)
- LPUART (Low-Power UART) for serial communication and debug
    - Standard functionality with MODEM/IrDA (FEATURE_EN = 2)
    - TX FIFO size of 32 entries (TXFIFO_SZ = 5)
    - RX FIFO size of 5(RXFIFO_SZ = 5)
- RGPIO (Rapid General-Purpose Input/Output) for fast pin I/O capability
    - Dual access (AIPS and AHB access from system peripheral address space)
- INTMUX (Interrupt Mux) to select local interrupts routed outside of the subsystem
- SEMA42 (hardware semaphore) for HMP synchronization to shared resources

Table 66: Cortex M4 GPIO Signals

Pin #	Pin Name	Ball
J3.34	M40_GPIO0_IO00	AR47
J3.29	M40_GPIO0_IO01	AU53
J3.38	M40_GPIO0_IO02	AM44
J3.32	M40_GPIO0_IO03	AU51
J3.40	M41_GPIO0_IO00	AP44
J1.11	M41_GPIO0_IO01	AU47
J1.9	M41_GPIO0_IO02	AR45
J3.36	M41_GPIO0_IO03	AU49

Table 67: Cortex M4 UART Signals

Pin #	Pin Name	Ball
J3.38	M40_UART0_RX	AM44
J3.32	M40_UART0_TX	AU51
J1.9	M41_UART0_RX	AR45
J3.36	M41_UART0_TX	AU49

Table 68: Cortex M4 I2C Signals

Pin #	Pin Name	Ball
J3.38	M40_I2C0_SCL	AM44
J3.32	M40_I2C0_SDA	AU51
J1.9	M41_I2C0_SCL	AR45
J3.36	M41_I2C0_SDA	AU49

Table 69: Cortex M4 Timer and PWM Module Signals

Pin #	Pin Name	Ball
J3.34	M40_TPM0_CH0	AR47
J3.29	M40_TPM0_CH1	AU53
J3.40	M41_TPM0_CH0	AP44
J1.11	M41_TPM0_CH1	AU47

8.23 General Purpose IO

The SOM provides IO pins which can be used as GPIOs. See Chapter 5 for a complete SOM connectors' signal list and GPIO multiplexing.

9 Power

9.1 VBAT

The SOM is supplied with a battery voltage of: 3.3V - 5V.

Table 70: VBAT Power

Pin #	Pin name
J3.69	VBAT
J3.70	VBAT
J3.71	VBAT
J3.72	VBAT
J3.73	VBAT
J3.74	VBAT
J3.75	VBAT
J3.76	VBAT
J3.77	VBAT
J3.78	VBAT
J3.79	VBAT
J3.80	VBAT
J3.81	VBAT
J3.82	VBAT
J3.83	VBAT
J3.84	VBAT
J3.85	VBAT
J3.86	VBAT
J3.87	VBAT
J3.88	VBAT
J3.89	VBAT
J3.90	VBAT

9.2 VCOIN

The SOM uses 3.0V Lithium cell for the following purpose:

- RTC supply VSNVS 1.8V/3.0 V/3.3V.
- Battery backed memory.

Table 71: VCOIN Power

Pin #	Pin name
J4.29	VCOIN

9.3 HSIC Power

To use HSIC subsystem the SOM should be powered by 1.2V power supply via the below pin.
If there is no use for HSIC subsystem, it can be powered by 1.8V and 3.3V as needed.

Table 72: HSIC Power

Pin #	Pin name
J4.19[5]	VCC_HSIC

9.4 Output Power Supplies

The SOM exposes two general purpose switching power supplies of 3.3V/200mA and 1.8V/200mA.
In addition, the SOM exposes two general purpose LDO of 1.5V-5V one 200mA and second 400mA.

Table 73: 1.8V/200mA power supply pins

Pin #	Pin name
J3.68	SW_1P8

Table 74: 3.3V/200mA power supply pins

Pin #	Pin name
J3.67	SW_3P3

Table 75: 1.5-5V/200mA power supply pins

J4.52	P2_LDO3
J4.54	P2_LDO3

Table 76: 1.5-5V/400mA power supply pins

Pin #	Pin name
J4.48	P2_LDO4
J4.50	P2_LDO4

9.5 Ground Connections

Table 77: Digital Ground Pins

Pin #	Pin name
J1.13, J1.18, J1.24, J1.39, J1.42, J1.48, J1.57, J1.63, J1.66, J1.81, J1.87, J1.88, J2.17, J2.22, J2.23, J2.28, J2.35, J2.46, J2.52, J2.53, J2.59, J2.69, J2.70, J3.27, J3.28, J3.50, J3.51, J3.56, J3.59, J3.62, J4.12, J4.17, J4.18, J4.24, J4.25, J4.3, J4.30, J4.33, J4.39, J4.41, J4.49, J4.6, J4.77,	GND

9.6 Analog Ground Pin Used For Audio:

Table 78: Analog Ground Pins

Pin #	Pin name
J4.90	AGND

9.7 Boot Configuration

Table 79: SOM boot options

	SCU_DSC_BOOT_MODE5	SCU_DSC_BOOT_MODE3	SCU_DSC_BOOT_MODE2
Fuse boot	0	0	0
Serial Boot	0	0	1
eMMC Boot	0	1	0
SD Boot	0	1	1

10 Assembly Options

To make the solution as Flexible as possible the following assembly options were added. The assembly options help customers to order the SOM subversion that include only the needed interfaces with a lower cost.

10.1 LVDS1 Dual Channel

DSI interface and LVDS 1 Channel 1 interface share same SOM pins. The SOM can be ordered with LVDS1 CH1 option assembled. In this special configuration the DSI interface is not exposed and LVDS1 CH1 allows connecting dual 1080p LVDS displays to SOM.
Resistor networks RN3 and RN6 should be assembled to get DSI interface exposed. Resistor networks RN4 and RN5 should be assembled to get LVDS interface exposed.

Table 80: LVDS - DSI assembly option

Pin #	Default SOM option		Special SOM option	
	Pin name	Ball	Pin name	Ball
J1.20[4]	MIPI_DSI0_CLK_N	BN27	LVDS1_T1CLKP	BM34
J1.22[4]	MIPI_DSI0_CLK_P	BL27	LVDS1_T1CLKN	BK34
J1.28[4]	MIPI_DSI0_DATA0_N	BM28	LVDS1_T1AN	BL33
J1.26[4]	MIPI_DSI0_DATA0_P	BK28	LVDS1_T1AP	BN33
J1.32[4]	MIPI_DSI0_DATA1_N	BM26	LVDS1_T1BN	BK32
J1.30[4]	MIPI_DSI0_DATA1_P	BK26	LVDS1_T1BP	BM32
J1.36[4]	MIPI_DSI0_DATA2_N	BN29	LVDS1_T1CN	BL31
J1.34[4]	MIPI_DSI0_DATA2_P	BL29	LVDS1_T1CP	BN31
J1.40[4]	MIPI_DSI0_DATA3_N	BN25	LVDS1_T1DN	BK30
J1.38[4]	MIPI_DSI0_DATA3_P	BL25	LVDS1_T1DP	BM30
J1.76[4]	MIPI_DSI0_GPIO0_00	BD30	LVDS1_GPIO0_IO00	BD34
J1.78[4]	MIPI_DSI0_GPIO0_01	BD28	LVDS1_GPIO0_IO01	BH36
J1.70[4]	MIPI_DSI0_I2C0_SCL	BE29	LVDS1_I2C1_SCL	BD32
J1.68[4]	MIPI_DSI0_I2C0_SDA	BE31	LVDS1_I2C1_SDA	BN35

10.2 RGMII

The SOM can be ordered with RGMII interface exposed, this allows direct connection of external Ethernet Switch. In this special configuration Ethernet1 PHY is not assembled and the RGMII interface exposed on the same SOM pins.
By default, the voltage of these pins is 3.3V. Starting from PCB Revision 1.3 the voltage level can be changed to 1.8V to support standard RGMII voltage level.
The selection is done using GPIO2_IO27. Low level of this GPIO will select 3.3V, high level will select 1.8V.

Table 81: Ethernet - RGMII assembly option

Pin #	Default SOM option		Special SOM option	
	Pin name	Ball	Pin name	Ball
J3.22[2]	ETH1_LED_LINK_10_100	AR8033.24	ENET1_RGMII_TXC	D46
J3.20[2]	ETH1_LED_LINK_1000	AR8033.26	ENET1_RGMII_TXD2	G47
J3.18[2]	ETH1_LED_ACT	AR8033.23	ENET1_RGMII_TX_CTL	B48
J3.4[2]	ETH1_MDI_A_M	AR8033.12	ENET1_RGMII_RXD2	D52
J3.2[2]	ETH1_MDI_A_P	AR8033.11	ENET1_RGMII_TXD0	A49
J3.8[2]	ETH1_MDI_B_M	AR8033.15	ENET1_RGMII_TXD1	C47
J3.6[2]	ETH1_MDI_B_P	AR8033.14	ENET1_RGMII_RXD3	E53
J3.12[2]	ETH1_MDI_C_M	AR8033.18	ENET1_RGMII_RX_CTL	E49
J3.10[2]	ETH1_MDI_C_P	AR8033.17	ENET1_RGMII_RXC	B50
J3.16[2]	ETH1_MDI_D_M	AR8033.21	ENET1_RGMII_RXD1	C51
J3.14[2]	ETH1_MDI_D_P	AR8033.20	ENET1_RGMII_RXD0	E51
J3.31[2]	NC		ENET1_RGMII_TXD3	D48

10.3 Analog Audio Codec

The SOM can be ordered without Audio Codec chip assembled; it allows reducing the overall cost of the product in case the Analog Audio is not used.

10.4 Ethernet PHY0

The SOM can be ordered without Ethernet0 PHY chip assembled, it allows reducing the overall cost of the product in case the Ethernet Interfaces are not used.

10.5 LPDDR4

The SOM can be ordered with different RAM size capacities, it allows reducing the overall cost of the product in case lower RAM size is sufficient.

10.6 eMMC

The SOM can be ordered with different eMMC size capacities, it allows reducing the overall cost of the product in case lower eMMC size is sufficient.

10.7 Bluetooth

The SOM can be ordered with UART1 interface accessible. In this case the Bluetooth interface will not be available. For testing purposes same operation can be achieved by pulling GPIO4_IO26 high. It will disable ON-SOM level translator and allow UART1 operation.

11 Electrical Specifications

11.1 Absolute Maximum Ratings

Table 82: Absolute Maximum Ratings

Pin #	Min	Max	Units	Comments
VBAT	-0.3	6	V	
VCOIN	-0.3	5.5	V	
USB_OTG1_VBUS	-0.3	5.5	V	OTG1 and OTG2 are implemented differently, requiring different specifications.
USB_OTG1_ID	-0.3	1.98	V	
USB_OTG2_DP/USB_OTG2_DN	-0.3	3.63	V	
USB_OTG2_VBUS	-0.3	3.63	V	This pin is not 5V tolerant. Use an external voltage divider for this VBUS connection.
USB_OTG2_ID	-0.3	3.63	V	
USB3.0 pins		1.2	Vp-p	Maximum differential input voltage
USB-HSIC pins	-0.3	1.5 V		
MIPI_CSI pins	-0.15	1.45 V		
MIPI_DSI pins	-0.15	1.45 V		
LVDS pins	-0.15	1.45 V		
HDMI-RX pins	-0.15	1.2	Vp-p	Differential input voltage
ESD damage immunity Human Body Model (HBM) Charge Device Model (CDM)	—2000	250	V	PCIe/SATA, HDMI-RX andTX, USB3 interfaces are 1000V HBM instead of 2000V

11.2 Operating Conditions

Table 83: Operating Ranges

Parameter	Min.	Typ.	Max.	Unit
VBAT			5.5	V
VCOIN			4.2	V

11.3 Power Consumption

Table 84: SPEAR-MX8 Power Consumption

Mode	Voltage	Current	Power	Conditions
Run	3.7V	0.95A	3.15W	Idle
Run	3.7V	1.16A	4.3W	Linux up, Wi-Fi connected and IPERF3 is running in 802.11 n 2.4GHz
Run	3.7V	1.25A	4.6W	Linux up, Wi-Fi connected and IPERF3 is running in 802.11 n 5.0GHz
Run	3.7V	1.25A	4.6W	Camera Preview
Run	3.7V	1.55A	5.7W	H264 playback
Standby	3.7V	1.61A	6W	H264 record

12 Environmental Specifications

Table 85: Environmental Specifications

Parameter	Min	Max
Extended Operating Temperature Range	-25°C	85°C
Industrial Operating Temperature Range	-40°C	85°C
Storage temperature	-40°C	85°C
Relative humidity (operation)	10%	90%
Relative humidity (storage)	05%	95%
Referring MIL-HDBK-217F-2 Parts Count Reliability Prediction Method Model:		
50°C, Class B-1, GM	121K hrs.	
50°C, Class B-1, GB	1400K hrs.	

13 Mechanical Drawings

13.1 Carrier Board Mounting

The SOM has four mounting holes for mounting it to the carrier board which are plated holes and connected to GND.

13.2 Standoffs

Customers requiring a mechanical solution for mounting in harsh vibration environments can use the following standoff:

Manufacturer: **MAC8**

PN: **TH-1.6-1.5-M2**

13.3 Thermal Management

To handle intensive applications where thermal management is required, Variscite offers a heat spreader:

Variscite PN: **TBD**

The heat spreader will allow the best solution to attach various heat sources on board to an additional passive or active solution will be required depending on the application.

13.4 SOM Dimensions

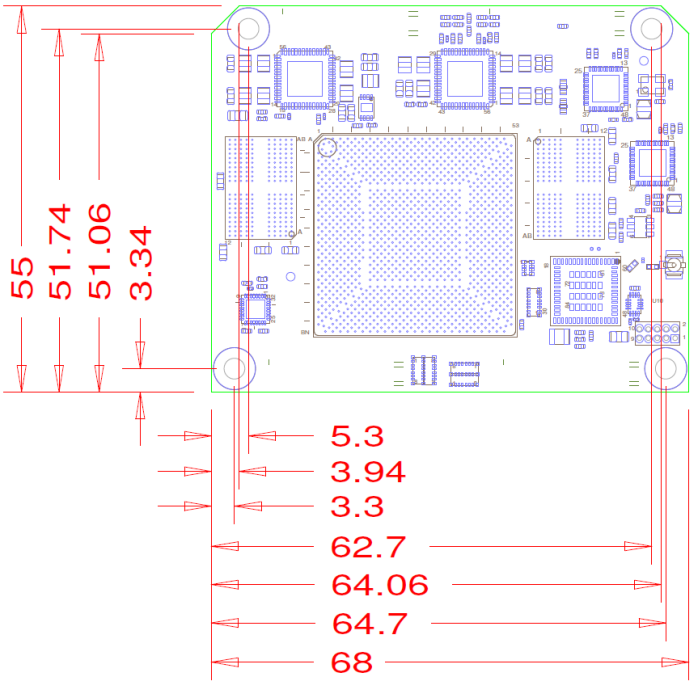


Figure 7: SPEAR-MX8 Top View Mechanics in millimeters

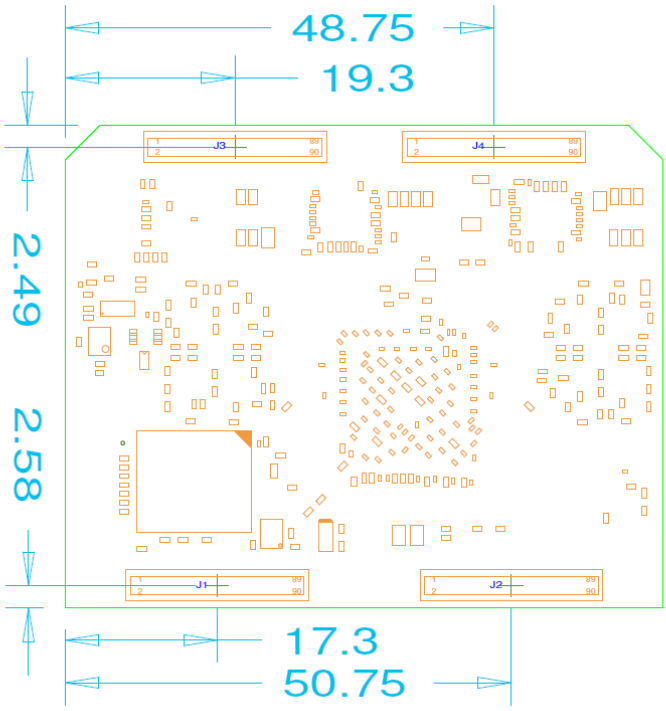


Figure 8: SPEAR-MX8 Bottom View Mechanics in millimeters

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