

VAR-DT8MCustomBoard



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**Disclaimer:**

SchematicS are for reference only.  
 Variscite LTD provides no warranty for the use of these schematics.  
 Schematics are subject to change without notice.

**Revision History**

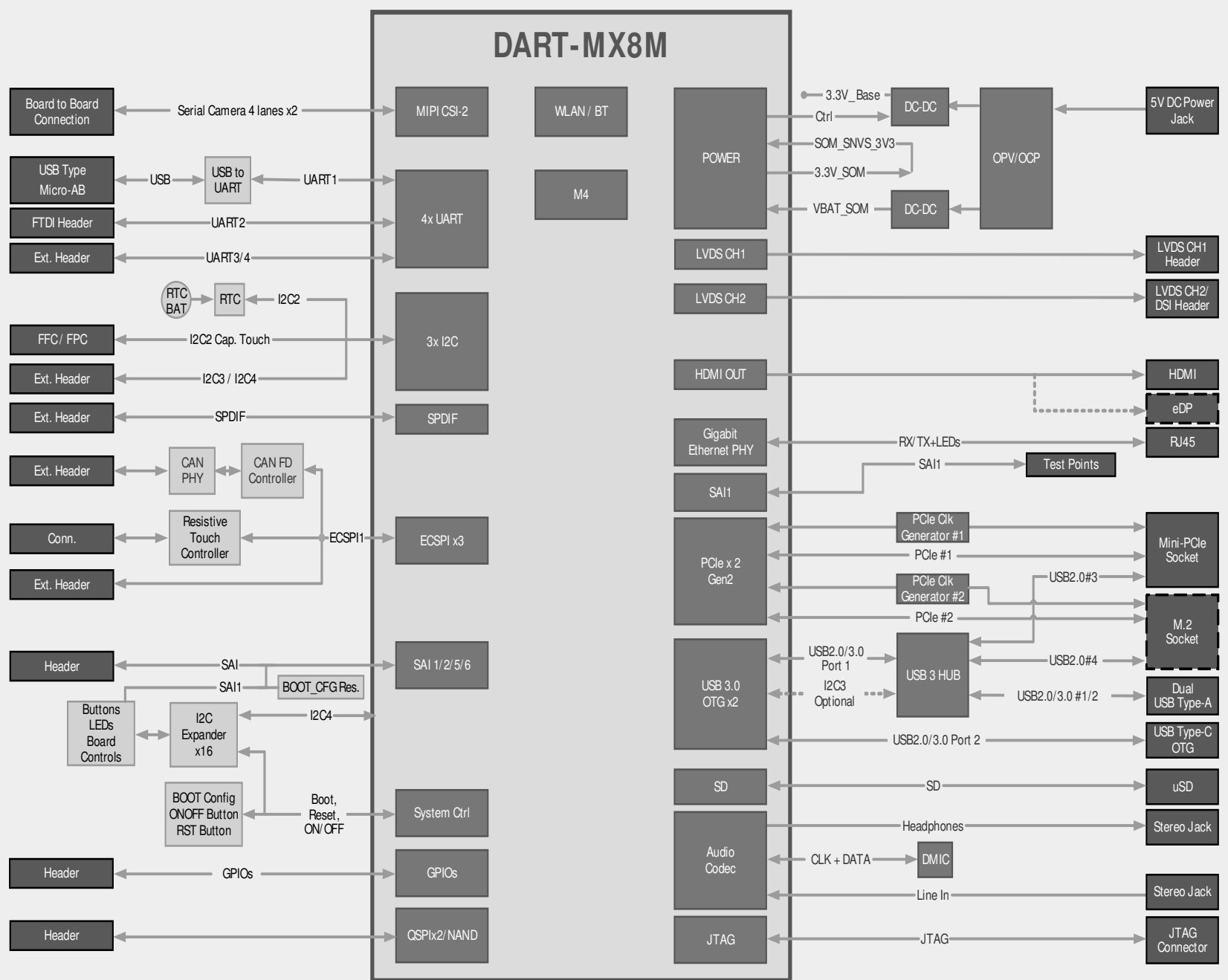
Document	Carrier	Description
1.0	2.0	Changes from DOC 1.9 Carrier 1.4D include: * Optimisation for DART-MX8MP: - Added external ethernet PHY - Control IOs used on previous version over SAI1 now controlled via I2C expander - Added DSI header option for DART-MX8MP stock item exposed pins; Pinout compatible to Symphony J7+J8 - Native USB ID usage added important note - USB Type C active discharge replaced with bleeder - USB Type C crossbar differential switch simplified. - Removed DT8M NAND option - Added QSPI header J41 - located in location of J25 - J27 & J28 pinout aligned to Symphony - Added PD on J1.38 for BSP CustomV2.0 signal. - Added additional CAN PHY on iMX8MP - U44 footprint modified from SOIC to DFN - SD card power switch modified - Main power switch type align to Symphony - DART-MX8M DP connector replaced with 40pin eDP REF. design - HDMI path simplified - PINMUX page deleted - reference to XLS - Aded reference design for 12Mb/s CAN-FD transceiver - Added M.2. PCIe reference design - Add option on bottom to route PCIe port 1 to M.2 connector - Replace boot config drivers to 3state type - Replace MCP2518 crystal to 40MHz and connect RX_INT - Updated Block Diagrams - VCC_SOM Increased to 3.8V (R145 changed to 18K) - D9, C58 Removed. VCC_BASE_3V3 goes up just after NVCC_3V3
1.1	2.1	* GPLED4 controlled via FET Q14 to support DART-MX8M-PLUS 1.8V voltage level * Updated GPIO expanders U56,U57 footprint * Added note for U53 recommended P/N
1.2	3.0	* Due to EOL: - Changed BOM P/N: U23,U45,U46,U56,U59,U57 - Added optional resistors R291-R294 - Changed Assembly: U31 Not assembled, R167 assembled - Changed Ethernet PHY to ADIN1300: Changed Ethernet2 schematics, Added R295 * Changed J5 P/N and schematics to support ADIN1300 PHYs * Updated comments on schematic nets * R94-R97, R114-R117 assembled with Ferrite Bead
1.3	3.0A	* Due to EOL: U60,U62 changed to NFL18ZT207H1A3D * Due to Allocation Problems: U45,U59 changed to SN65HVD232QDR
1.4	3.0B	* DART-MX95 Block Diagram & Connectors added
1.5	3.0C	* DART-MX93 Block Diagram & Connectors added * DART-MX91 Block Diagram & Connectors added
1.7	3.0C	* DART-MX95 Block Diagram & Connectors symbols updated
1.8	3.0C	* New Logo

Title: 01. Cover

Size: A3	Document Number: VAR-DT8MCustomBoard	Project: VAR-DT8MCustomBoard	Rev: 3.0C R1.7
Designer: Leonid S.	Date: Tuesday, August 05, 2025		Approved By: _____
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# VAR-DT8MCustomBoard V2.x

Doc rev 1.0



**I2C BUS ADDRESS:**

I2C1: Internal to SOM  
 I2C2: PU - 10K on U8  
 10K on custom  
 0x54 BOARD ID EEPROM Page0  
 0x55 BOARD ID EEPROM Page1  
 0x68 RTC  
 0x38 CAPACITIVE TOUCH CTRLR  
 0x3D USB-C CC Logic PTN5150AHXMP  
 0x3C CSI P1 Camera (1V8) OV5640

I2C3: PU - 5K on SOM  
 0x60 SOM - Int. power ctrl.  
 0x2D USB3 HUB  
 0xXX Header J12

I2C4: PU - 10K on U8  
 10K on custom  
 0x3C CSI P2 Camera (1V8) OV5640  
 0xXX Header J12  
 0xXX mPCIE J23 & J32

**Important Notes:**

1. Length match for HS signals according to SOM DS
2. USB routed as 90 ohm Diff pairs
3. PCIe/SATA routed as 85 ohm Diff pairs
4. LVDS routed as 100 ohm Diff pairs
5. Other fast changing signals routed as 50 ohm

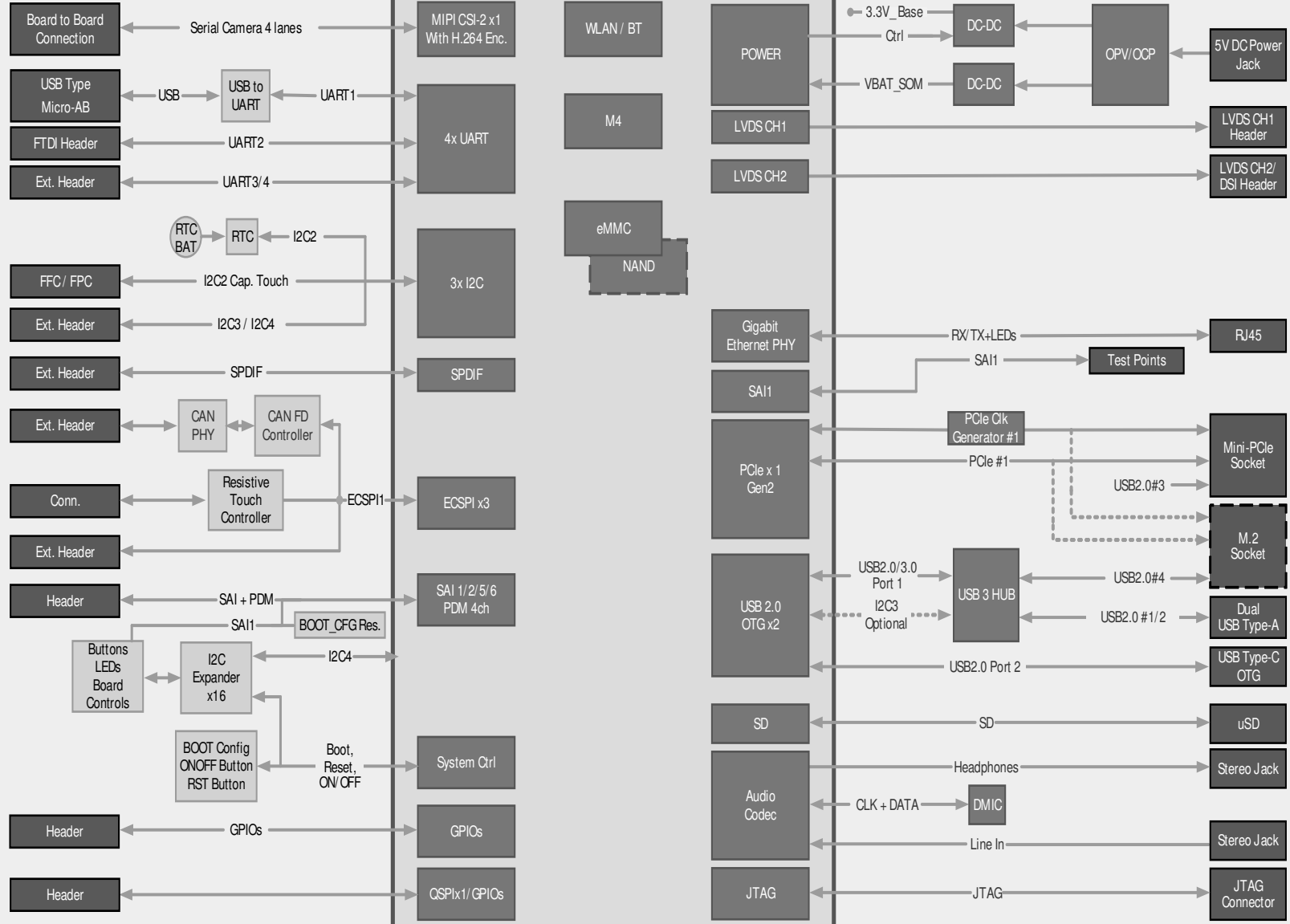
Title: 02A. Block Diagram with DART-MX8M

Size A3	Document Number VAR-DT8MCustomBoard	Project VAR-DT8MCustomBoard	Rev 3.0C R1.7
Designer: Leonid S.	Date: Tuesday, August 05, 2025	Approved By:	Sheet 2 of 17

# VAR-DT8MCustomBoard V2.x

Doc rev 1.0

## DART-MX8M-MINI



**I2C BUS ADDRESS:**

```

I2C1: Internal to SOM
I2C2: PU - 10K on U8
      10K on custom
      0x54 BOARD ID EEPROM Page0
      0x55 BOARD ID EEPROM Page1
      0x68 RTC
      0x38 CAPACITIVE TOUCH CTRLR
      0x3D USB-C CC Logic PTN5150AHXMP
      0x3C CSI P1 Camera (1V8) OV5640

I2C3: PU - 5K on SOM
      0x1A SOM - Int. CODEC
      0x2D USB3 HUB
      0xXX Header J12

I2C4: PU - 10K on U8
      10K on custom
      0x3C CSI P1 Camera (1V8) OV5640
      0xXX Header J12
      0xXX mPCIE J23 & J32
    
```

**Important Notes:**

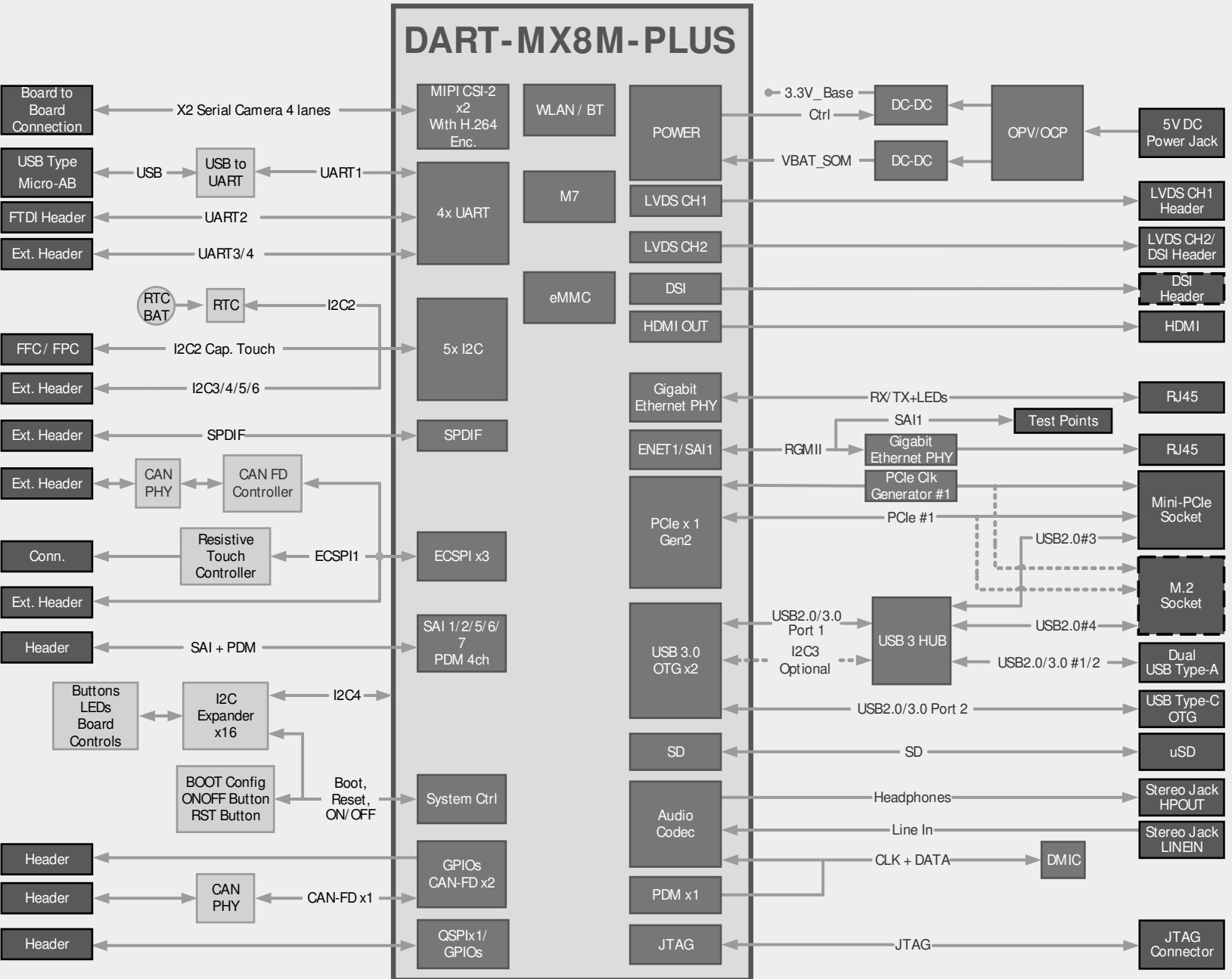
1. Length match for HS signals according to SOM DS
2. USB routed as 90 ohm Diff pairs
3. PCIe/SATA routed as 85 ohm Diff pairs
4. LVDS routed as 100 ohm Diff pairs
5. Other fast changing signals routed as 50 ohm



Title 02B. Block Diagram with DART-MX8M-MINI			
Size A3	Document Number VAR-DT8MCustomBoard	Project VAR-DT8MCustomBoard	Rev 3.0C R1.7
Designer Leonid S.	Date Tuesday, August 05, 2025	Approved By	Sheet 9 of 17

# VAR-DT8MCustomBoard V2.x

Doc rev 1.1



**I2C BUS ADDRESS:**

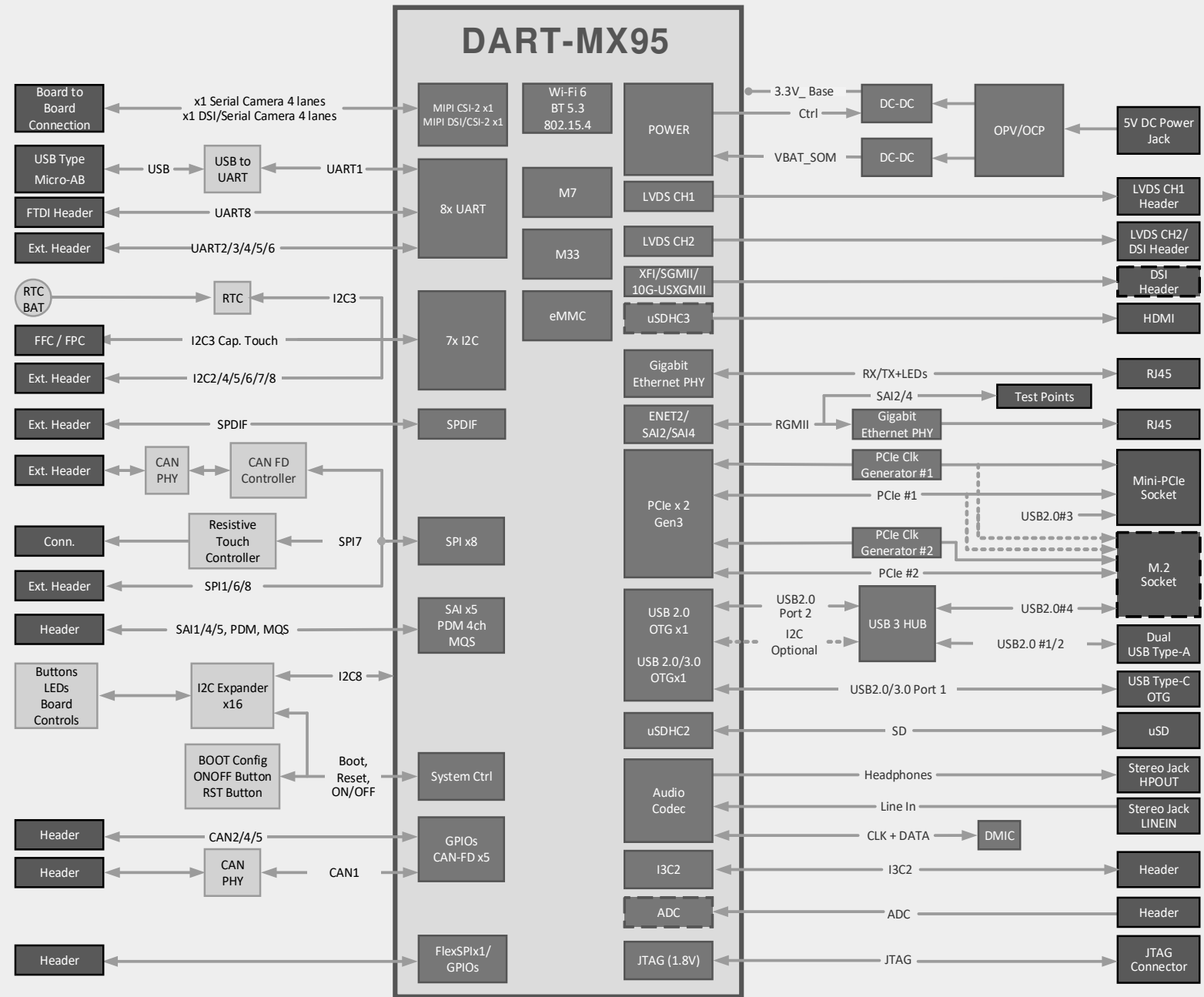
- I2C1: Internal to SOM
- I2C2: PU - 10K on U8  
10K on custom  
0x54 BOARD ID EEPROM Page0  
0x55 BOARD ID EEPROM Page1  
0x68 RTC  
0x38 CAPACITIVE TOUCH CTRLR  
0x3D USB-C CC Logic PTN5150AHXMP  
0x3C CSI P1 Camera (1V8) OV5640
- I2C3: PU - 5K on SOM  
  
0x2D USB3 HUB  
0xXX Header J12
- I2C4: PU - 10K on U8  
10K on custom  
0x3C CSI P1 Camera (1V8) OV5640  
0xXX Header J12  
0xXX mPCIe J23 & J32

**Important Notes:**

1. Length match for HS signals according to SOM DS
2. USB routed as 90 ohm Diff pairs
3. PCIe/SATA routed as 85 ohm Diff pairs
4. LVDS routed as 100 ohm Diff pairs
5. Other fast changing signals routed as 50 ohm

Title 02C. Block Diagram with DART-MX8M-PLUS			
Size A3	Document Number VAR-DT8MCustomBoard	Project VAR-DT8MCustomBoard	Rev 3.0C R1.7
Designer: Leonid S.		Approved By:	
Date: Tuesday, August 05, 2025		Sheet 4 of 17	

# VAR-DT8MCustomBoard V2.x Doc rev 1.1



**I2C BUS ADDRESS:**

I2C1: Internal to SOM  
 I2C2: PU - 10K on U8  
 10K on custom  
 0x54 BOARD ID EEPROM Page0  
 0x55 BOARD ID EEPROM Page1  
 0x68 RTC  
 0x38 CAPACITIVE TOUCH CTRLR  
 0x3D USB-C CC Logic PTN5150AHXMP  
 0x3C CSI P1 Camera (1V8) OV5640

I2C3: PU - 5K on SOM

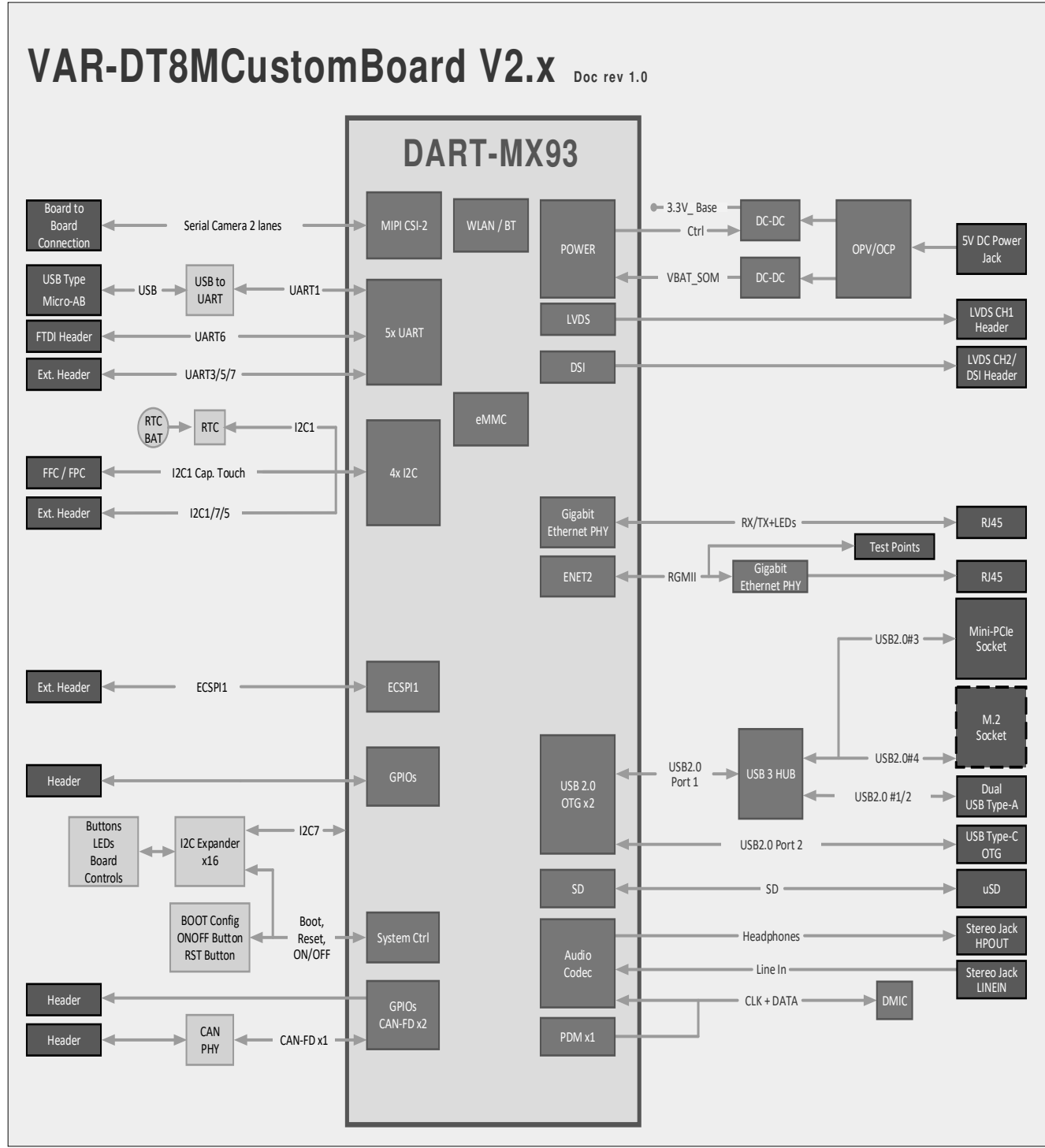
0x2D USB3 HUB  
 0xXX Header J12

I2C4: PU - 10K on U8  
 10K on custom  
 0x3C CSI P1 Camera (1V8) OV5640  
 0xXX Header J12  
 0xXX mPCIE J23 & J32

**Important Notes:**

1. Length match for HS signals according to SOM DS
2. USB routed as 90 ohm Diff pairs
3. PCIe/SATA routed as 85 ohm Diff pairs
4. LVDS routed as 100 ohm Diff pairs
5. Other fast changing signals routed as 50 ohm

Title 02D. Block Diagram with DART-MX95			
Size A3	Document Number VAR-DT8MCustomBoard	Project VAR-DT8MCustomBoard	Rev 3.0C R1.7
Designer Leonid S.	Date Tuesday, August 05, 2025	Approved By	Sheet 4 of 17



**I2C BUS ADDRESS:**

```

I2C3: Internal to SOM
I2C1: PU - 10K on U8
      10K on custom
      0x54 BOARD ID EEPROM Page0
      0x55 BOARD ID EEPROM Page1
      0x68 RTC
      0x38 CAPACITIVE TOUCH CTRLR
      0x3D USB-C CC Logic PTN5150AHXMP
      0x3C CSI P1 Camera (1V8) OV5640

I2C5: 0x2D USB3 HUB
      0xXX Header J12

I2C7: PU - 10K on U8
      10K on custom
      0x3C CSI P1 Camera (1V8) OV5640
      0xXX Header J12
      0xXX mPCIe J23 & J32
    
```

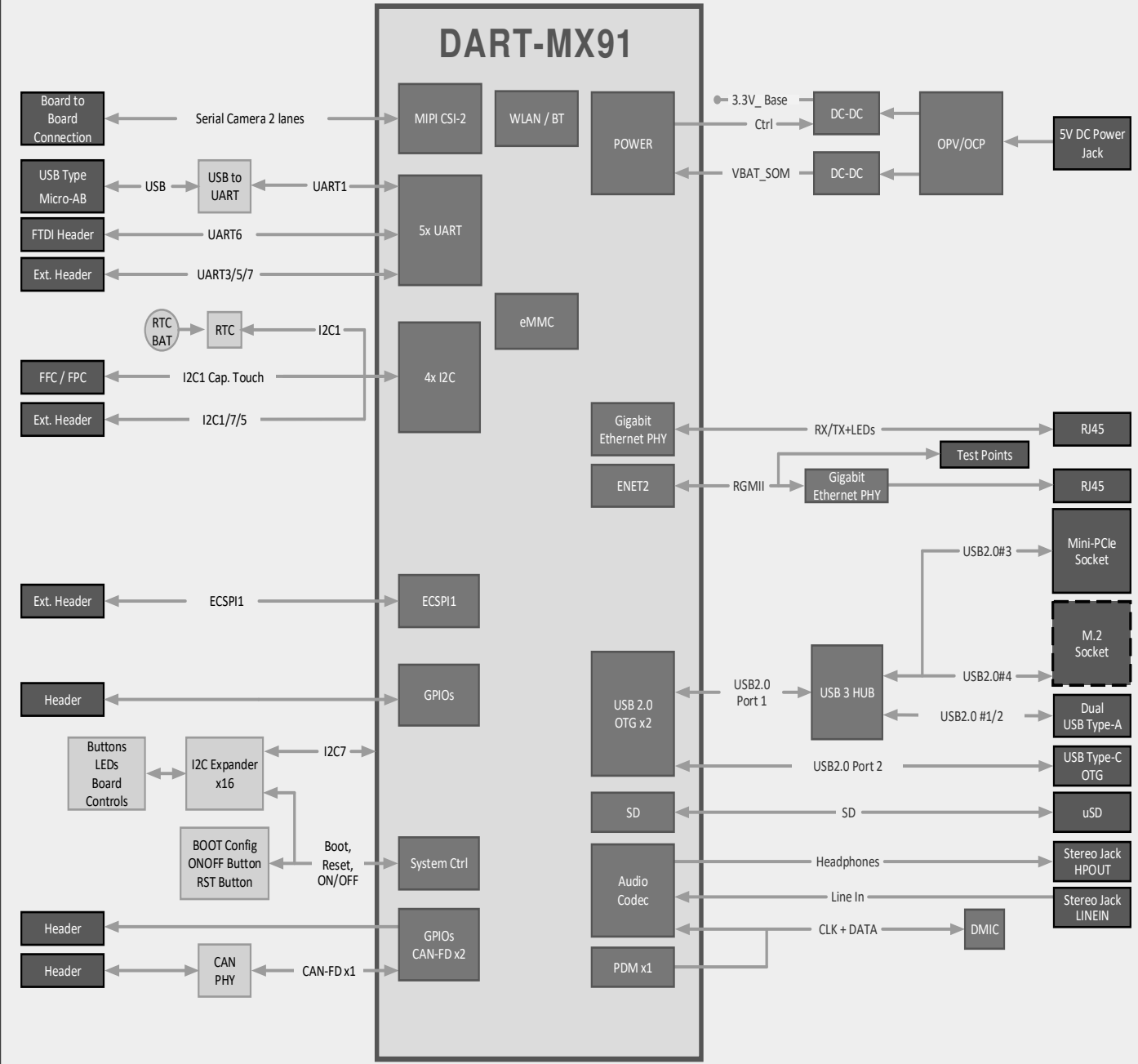
**Important Notes:**

1. Length match for HS signals according to SOM DS
2. USB routed as 90 ohm Diff pairs
3. LVDS routed as 100 ohm Diff pairs
3. Other fast changing signals routed as 50 ohm

Title 02E. Block Diagram with DART-MX93			
Size A3	Document Number VAR-DT8MCustomBoard	Project VAR-DT8MCustomBoard	Rev 3.0C R1.7
Designer Leonid S.	Date Tuesday, August 05, 2025	Approved By	Sheet 4 of 17

# 02F. Block Diagram - DART-MX91

## VAR-DT8MCustomBoard V2.x Doc rev 1.0



### I2C BUS ADDRESS:

- I2C3: Internal to SOM
- I2C1: PU - 10K on U8  
10K on custom  
0x54 BOARD ID EEPROM Page0  
0x55 BOARD ID EEPROM Page1  
0x68 RTC  
0x38 CAPACITIVE TOUCH CTRLR  
0x3D USB-C CC Logic PTN5150ARXMP  
0x3C CSI P1 Camera (1V8) OV5640
- I2C5: 0x2D USB3 HUB  
0xXX Header J12
- I2C7: PU - 10K on U8  
10K on custom  
0x3C CSI P1 Camera (1V8) OV5640  
0xXX Header J12  
0xXX mPCIe J23 & J32

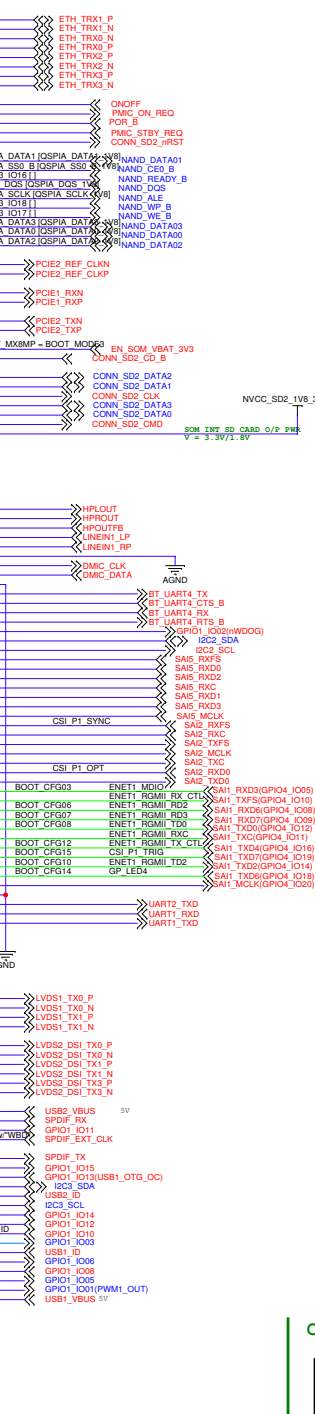
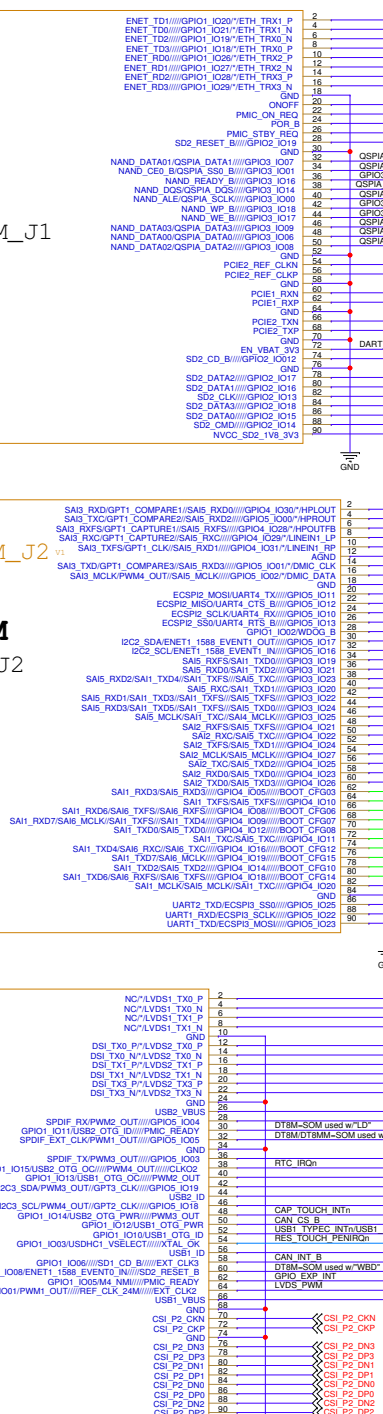
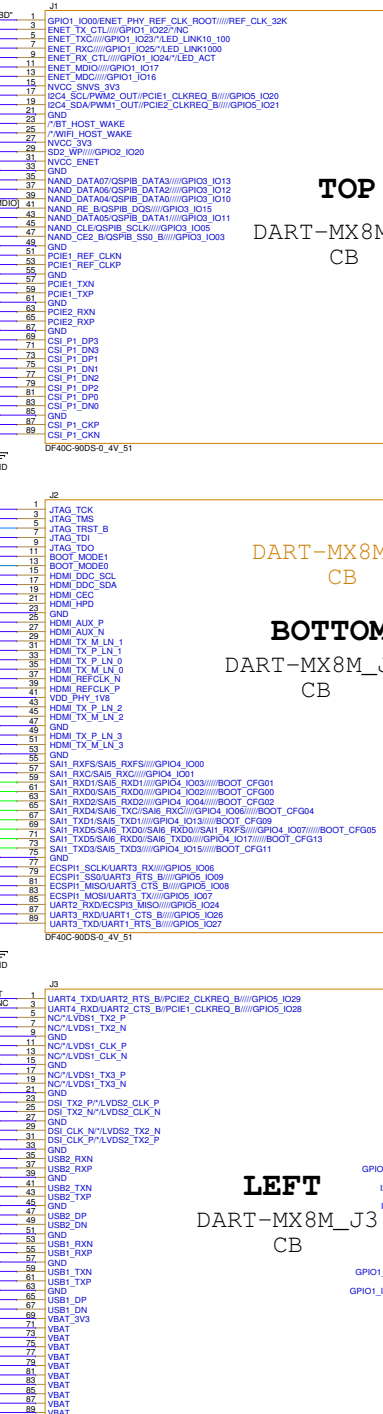
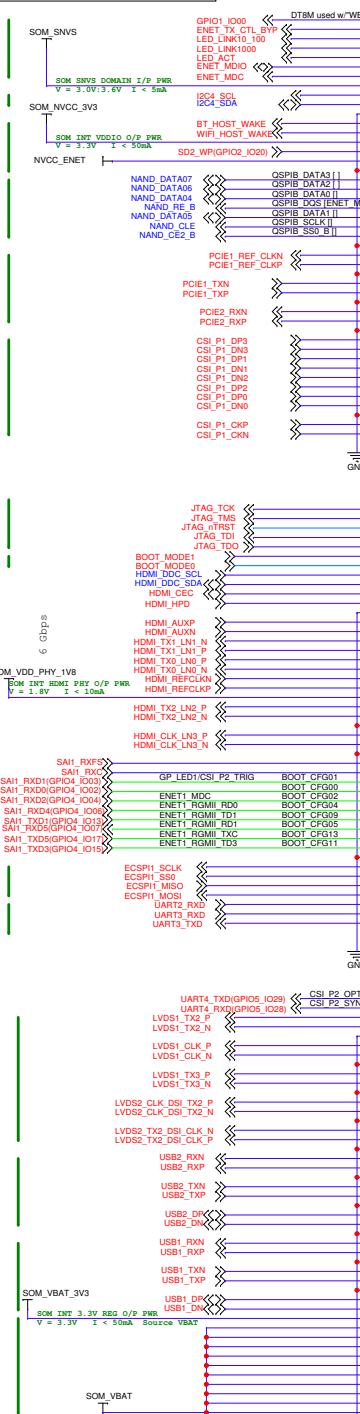
### Important Notes:

1. Length match for HS signals according to SOM DS
2. USB routed as 90 ohm Diff pairs
3. LVDS and DSI not exist. Headless mode only.
3. Other fast changing signals routed as 50 ohm



Title 02F. Block Diagram with DART-MX91			
Size A3	Document Number VAR-DT8MCustomBoard	Project VAR-DT8MCustomBoard	Rev 3.0C R1.7
Designer: Date:	Leonid S. Tuesday, August 05, 2025	Approved By: Sheet	4 of 17

ETH/MDIO
I2C4
WIFI HOST WAKE
QSPI B/NAND
PCIE
CSII
JTAG
BOOT MODE
HDMI
SAI1 BOOT CFG
ECSP11
UART
LVDS/DSI
USB2
USB1
SOM VBAT



ETH/MDIO
CTRL: ON/OFF, POR, PMIC\_ON, PMIC\_STBY
QSPI A/NAND
PCIE
SD2 WiFi Shared
CODEC/SAI3
UART4 Shared w/BT
WDG + I2C2
SAI5 RX
SAI2 RX/TX
SAI1 BOOT CFG
UART
LVDS/DSI
SPDIF
GPIO1
CSII



For complete alternate function per pin and specific SOM: please refer to "DART\_Compatibility\_and\_Pinout.XLS" located at: ftp://ftp.variscite.com/DART\_Compatibility

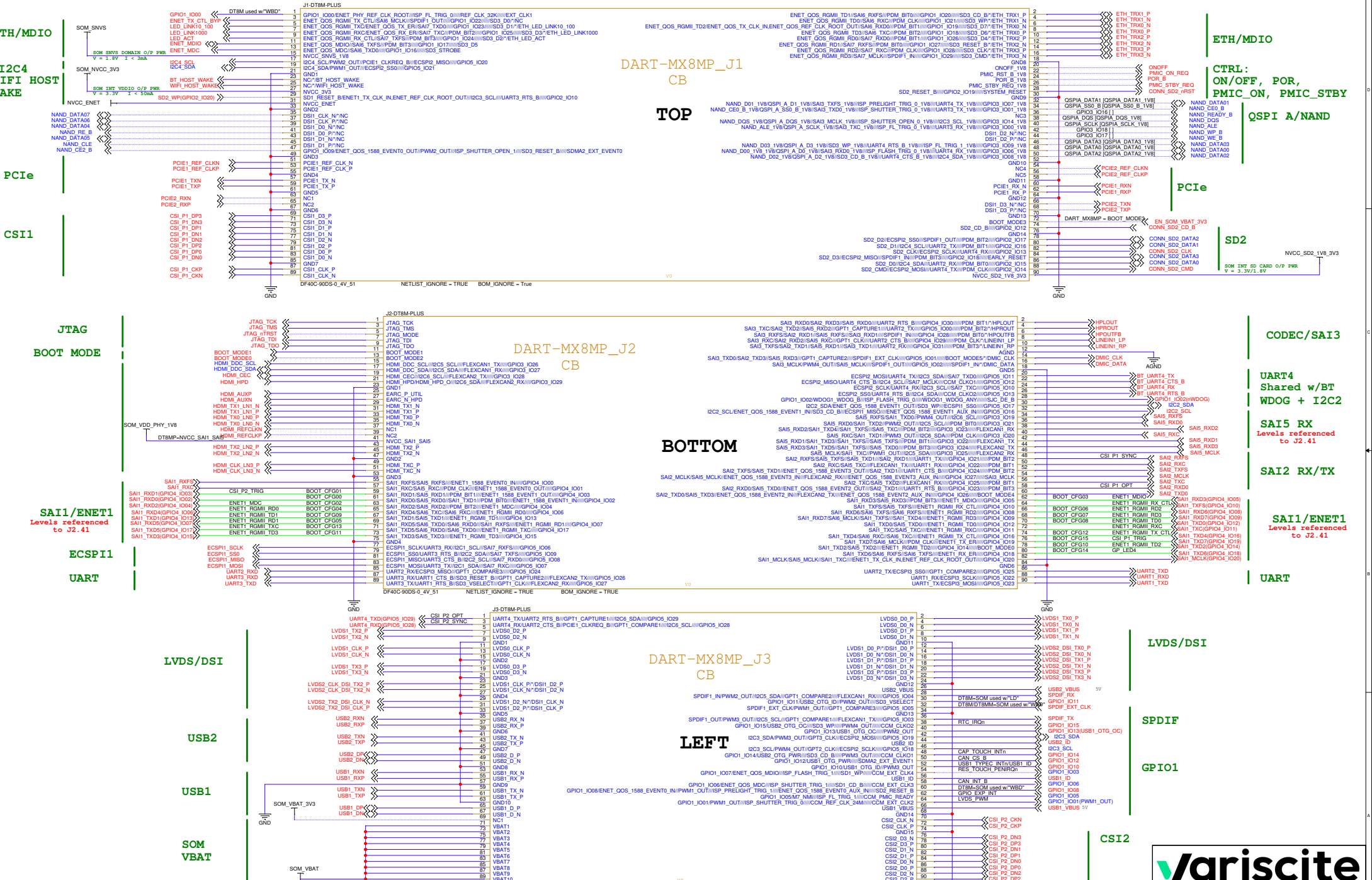
Note: Pinname with /\*/ prefix denotes a HW assy option.

Table with 4 columns: Title, Document Number, Project, Rev. Row 1: 03, DART-MX8M, VAR-DTBM, 3.0C R1.7. Row 2: Designer: Leonid S., Approved By: [blank]. Row 3: Date: Tuesday, August 05, 2025, Sheet: 5 of 17.



03C - DART-MX8M-PLUS

\*\*\* Dotted nets - Functionality differ from DART-MX8M. \*\*\*



For complete alternate function per pin and specific SOM:  
 please refer to "DART Compatibility and Pinout.XLS" located at:  
[ftp://ftp.variscite.com/DART\\_Compatibility](ftp://ftp.variscite.com/DART_Compatibility)

Note: Pinname with /\*/ prefix denotes a HWassy option.

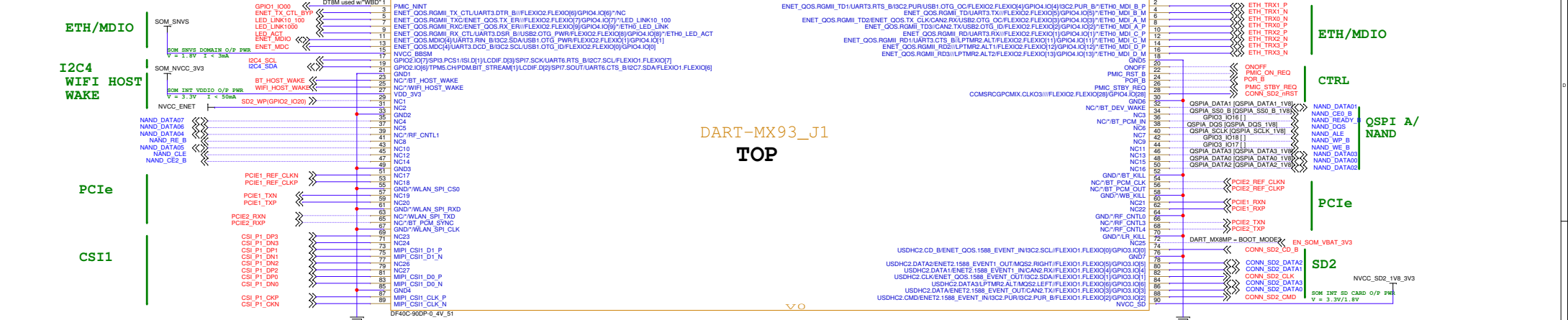


Title: 03C - DART-MX8M-PLUS			
Size: A2	Document Number: VAR-03C-001	Project: VAR-03C-001	Rev: 1.0
Designer: Leonid S.	Date: Tuesday, August 05, 2025	Approved By: [Signature]	Sheet: 7 of 17

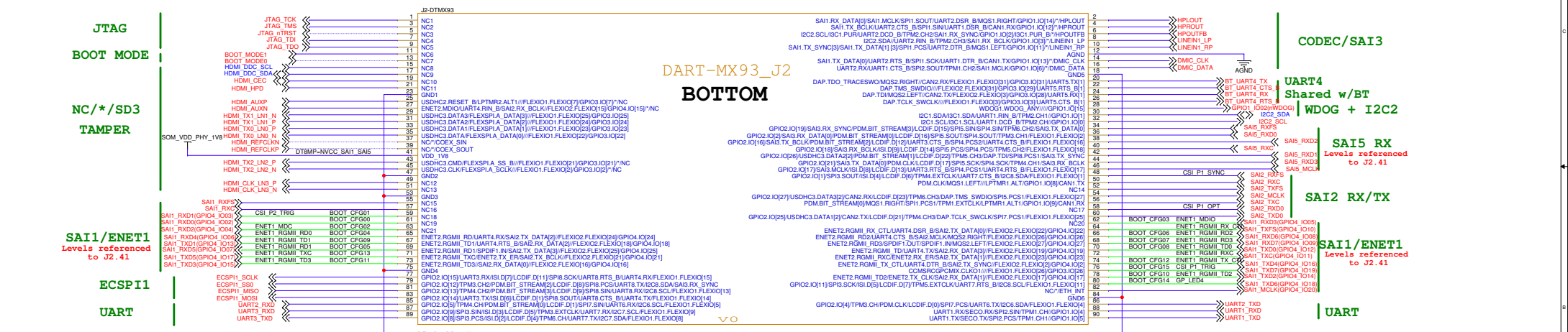


03E. DART-MX93

\*\*\* Dotted nets - Functionality differ from DART-MX8M. \*\*\*



DART-MX93\_J1 TOP



DART-MX93\_J2 BOTTOM



DART-MX93\_J3 LEFT

For complete alternate function per pin and specific SOM: please refer to "DART Compatibility and Pinout.XLS" located at: ftp://ftp.variscite.com/DART\_Compatibility

DF40C-90DP-0\_4V\_51

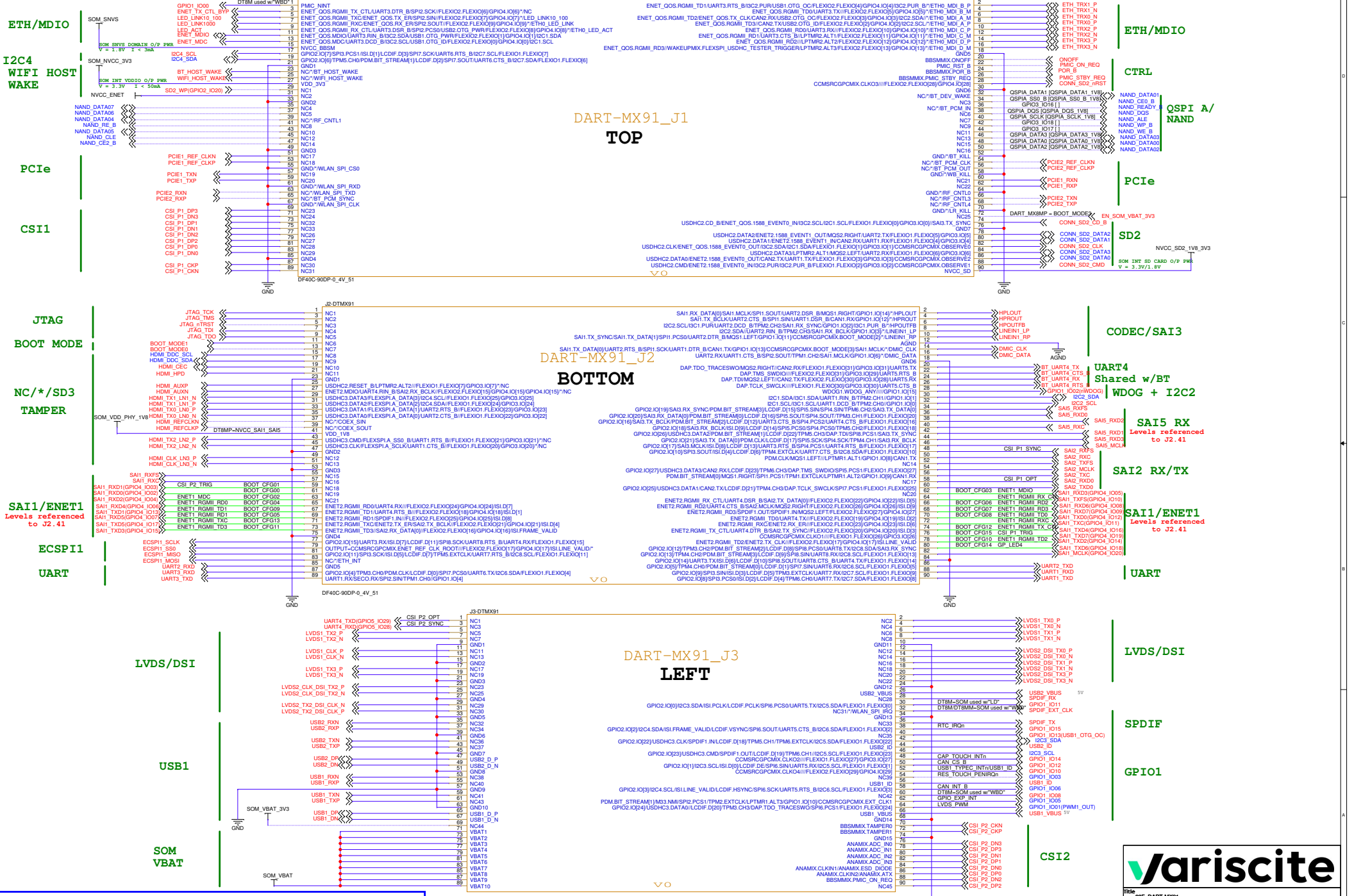
Note: Pinname with /\*/ prefix denotes a HW assy option.



Table with 4 columns: Title, Size A2, Document Number, Project, VAR-DT8M-CustomBoard, Date, Tuesday, August 05, 2025, Approved By, Sheet, 7 of 17

03F. DART-MX91

\*\*\* Dotted nets - Functionality differ from DART-MX8M. \*\*\*



For complete alternate function per pin and specific SOM, please refer to "DART Compatibility and Pinout.XLS" located at: ftp://ftp.variscite.com/DART\_Compatibility

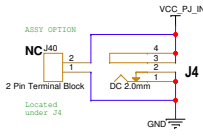
Note: Pinname with /\*/ prefix denotes a HW assy option.



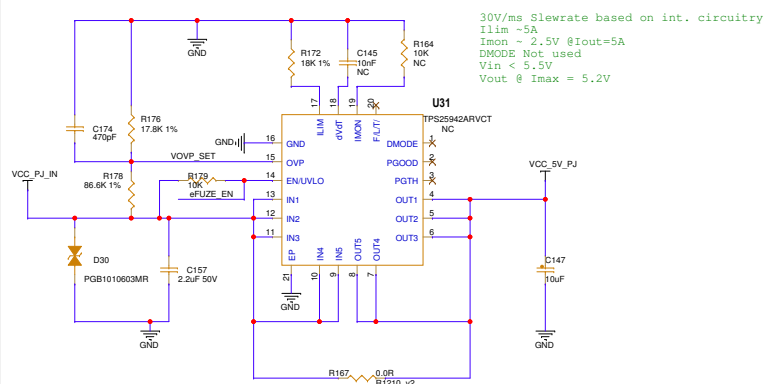
Title: 03F. DART-MX91			
Size A2	Document Number	Project	Rev
	VAR-DT8MCustomBoard	VAR-DT8MCustomBoard	3.0C R1.7
Designer:	Leonid S.	Approved By:	
Date:	Tuesday, August 05, 2025	Sheet:	7 of 17

# 04. Power, RTC, Board ID

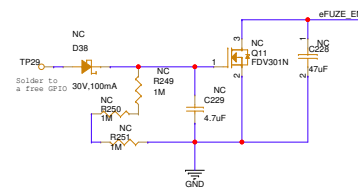
## 5VDC/4A POWER JACK



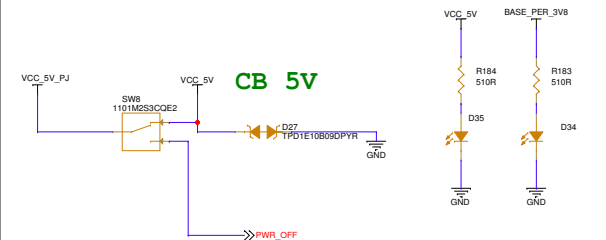
## PWR JACK 5V IN OVP/OCV



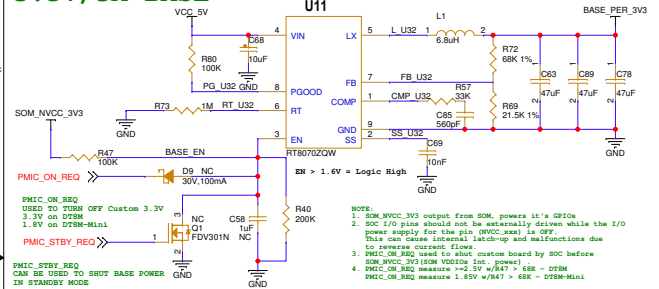
## Variscite Internal use circuit.



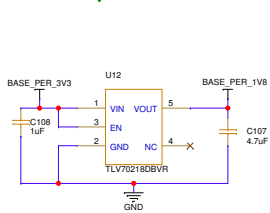
## POWER SW/ (ON/OFF)



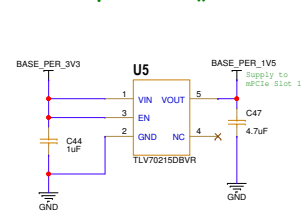
## 3.3V/3A BASE



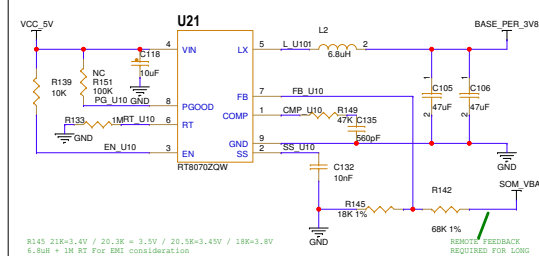
## 1.8V/0.3A BASE



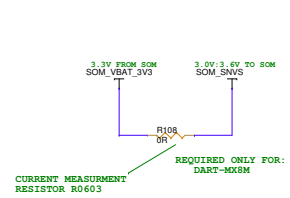
## 1.5V/0.3A #1 BASE



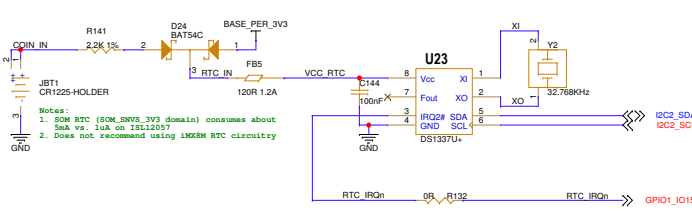
## 3.8V/3A FROM PWR JACK



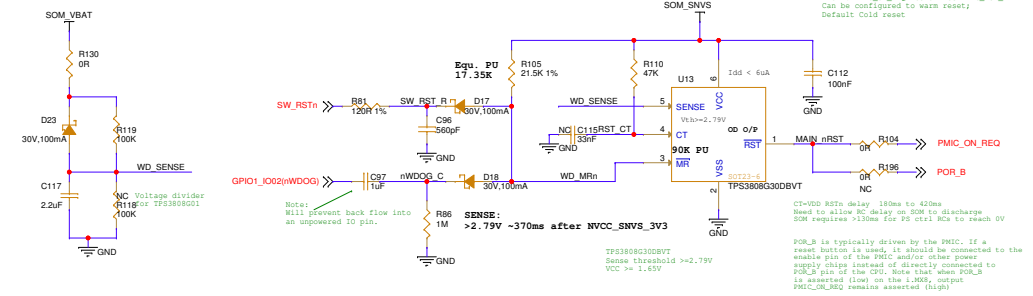
## SOM SNVS



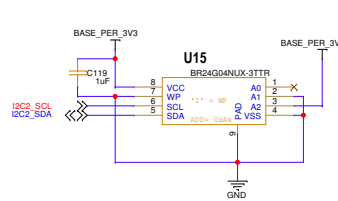
## RTC BATTERY



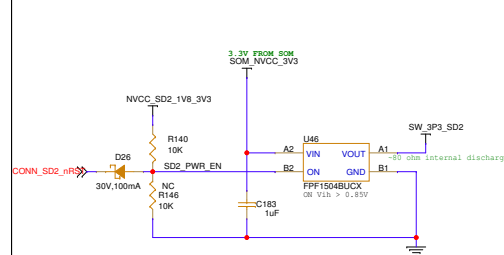
## RESET & WATCHDOG



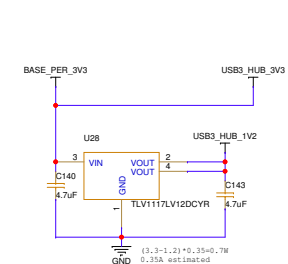
## BOARD ID



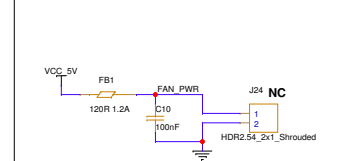
## SD POWER



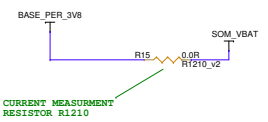
## USB3 HUB POWER



## FAN : 5V/0.2A



## SOM PWR



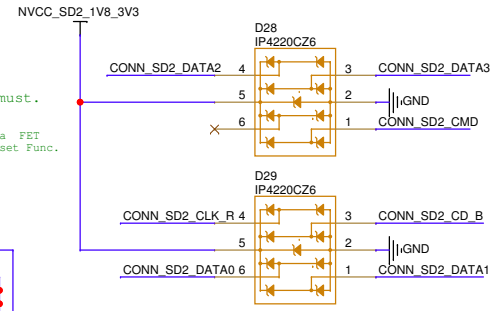
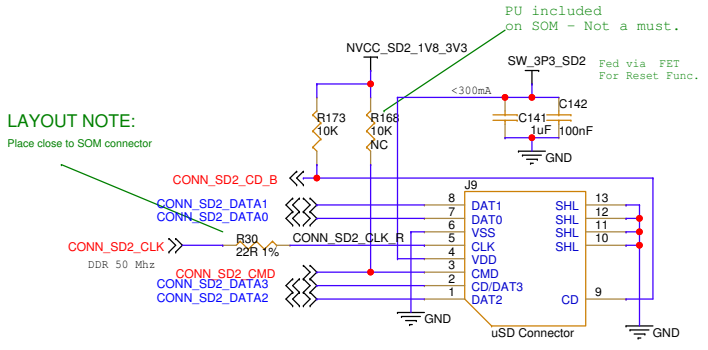
File: 04. Power, RTC, Board ID			
Size: VAR-DT8MCustomBoard	Document Number: VAR-DT8MCustomBoard	Project: VAR-DT8MCustomBoard	Rev: 3.0C R1.7
Designer: Leonid S.	Date: Tuesday, August 05, 2025	Approved By: Sheet 8 of 17	

# 05. ETH, uSD, AUDIO, MIPI-CSI

## uSD CARD

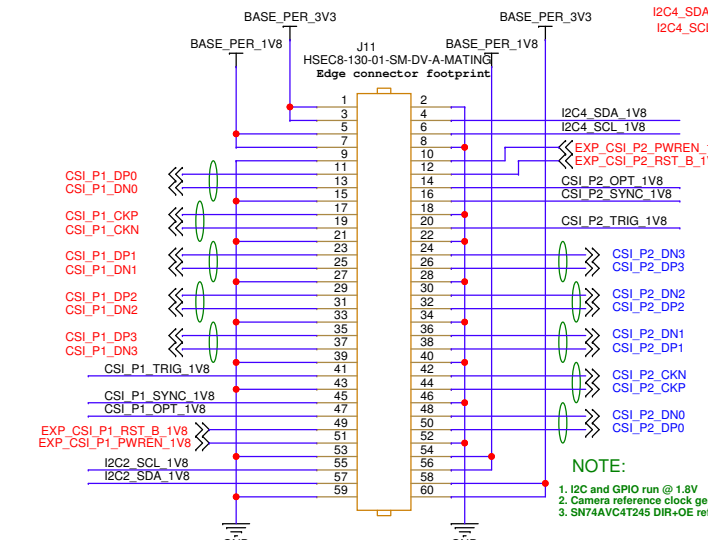
SDR104

**LAYOUT NOTE:**  
Place close to SOM connector



## MIPI-CSI0 + MIPI-CSI1

Connects to VariScite Custom MIPI-CSI2 Camera Board Qualified with x2 OV5640.

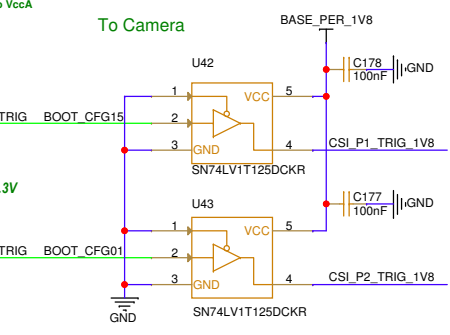


**LAYOUT NOTE:**  
Differential Impedance: 100 ohms  
SE 50 ohms  
HS mode: DIFF  
LP mode: SE  
Lane rate 1.5Gbps

**NOTE:**  
1. I2C and GPIO run @ 1.8V  
2. Camera reference clock generated on camera board  
3. SN74AVC4T245 DIR+OE ref'd to Vcca

From Camera  
SAI2\_RXFS  
SAI2\_RXD0  
SAI2\_RXD1  
UART4\_RXD(GPIO5\_IO28)  
UART4\_TXD(GPIO5\_IO29)

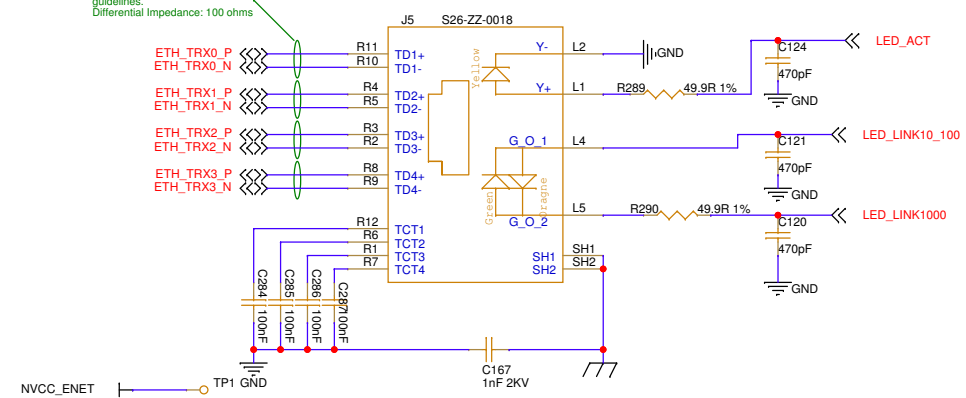
**Note:**  
Camera control signals shared with Header  
To use on the header disable buffer.  
Please enable Pullup in DTS



## LAYOUT NOTE:

Giga Ethernet Differential Pair.  
Follow Giga Ethernet routing guidelines.  
Differential Impedance: 100 ohms

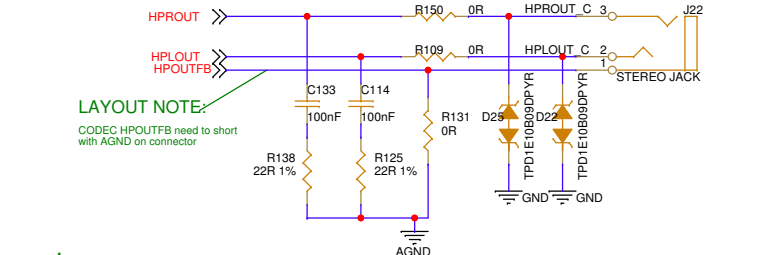
## Gigabit Ethernet (Internal)



**NOTE:** In case no "EC" on SOM  
Must feed NVCC\_ENET with either 1.8/2.5/3.3V

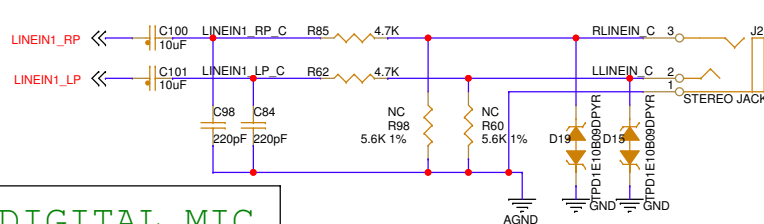
## AUDIO

## Headphones

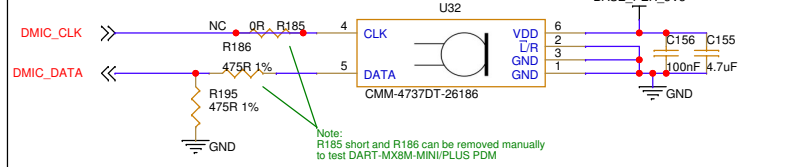


**LAYOUT NOTE:**  
CODEC HPOUTFB need to short with AGND on connector

## Line In



## DIGITAL MIC



Title 05. ETH, uSD, AUDIO, MIPI-CSI			
Size A3	Document Number VAR-DT8MCustomBoard	Project VAR-DT8MCustomBoard	Rev 3.0C R1.7
Designer Leonid S.	Date Tuesday, August 05, 2025	Approved By	Sheet 9 of 17

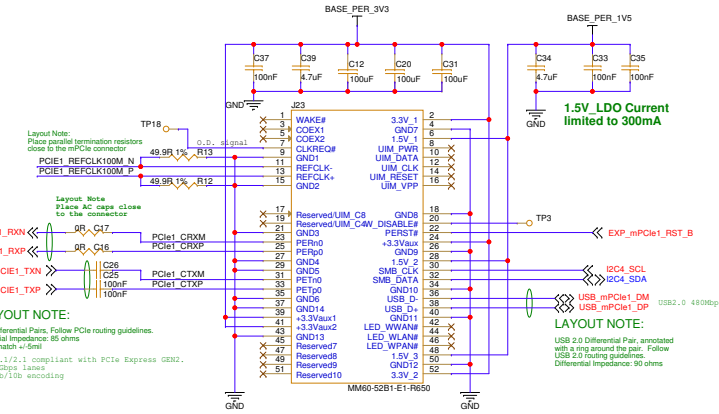
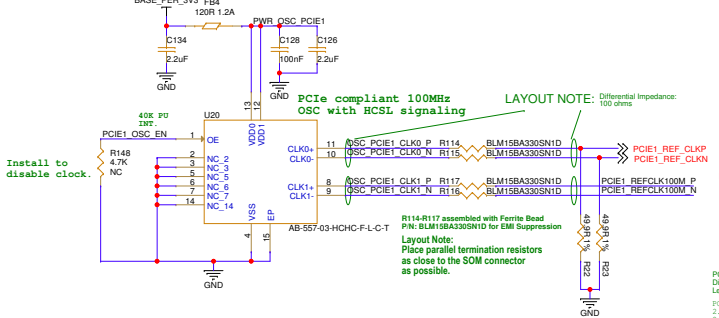


# 07. PCIe, QSPI, MIPI-DSI, USB DEBUG

Customboard 5V power supply is limited to 3A, shared with Board's USB devices. Do not connect devices which exceed current limitation.

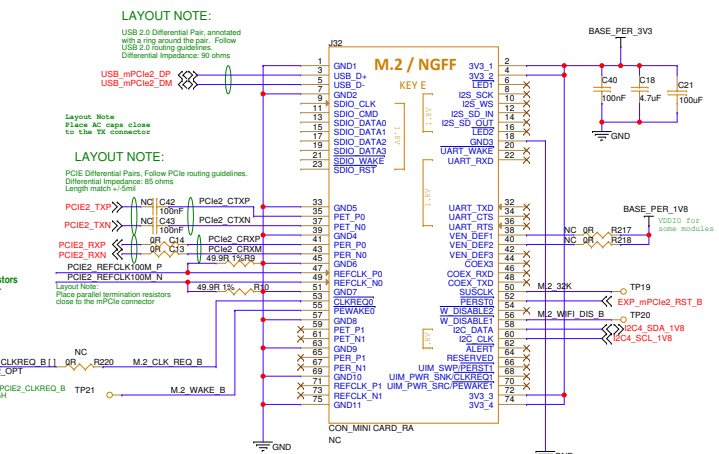
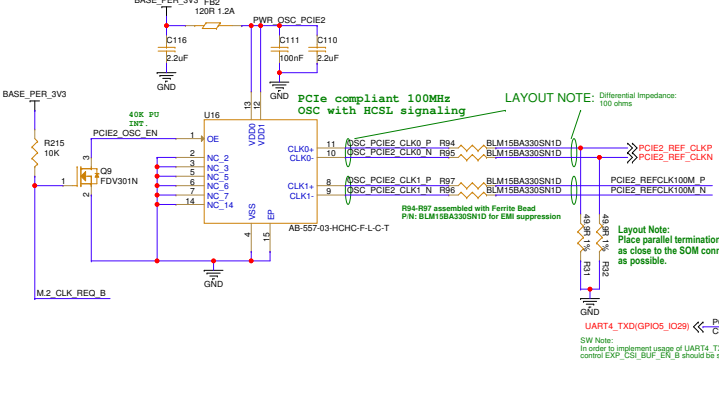
## mPCIexp CS

### PCIe CLK DIST.

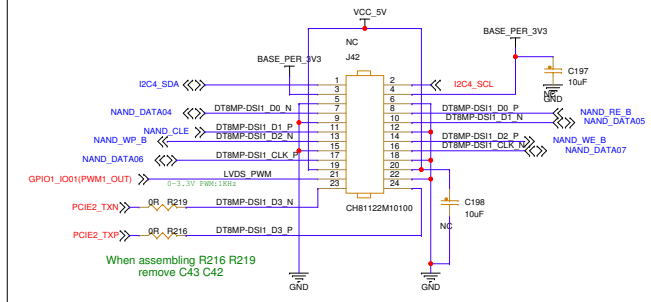


## M.2. ON PS - [Reference Design]

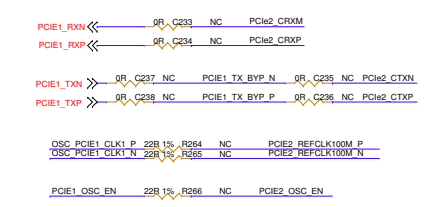
### PCIe CLK DIST.



## DART-MX8MP MIPI-DSI ON PS Compatible to Symphony J7+J8



## PCIe1 TO M.2 PATH



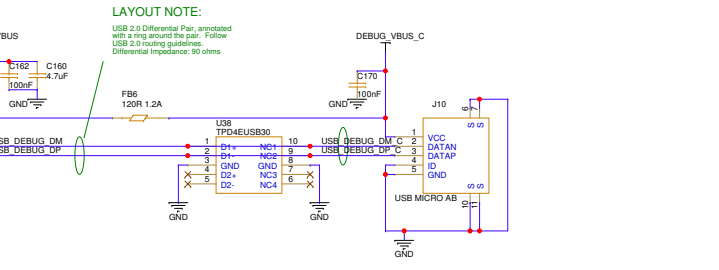
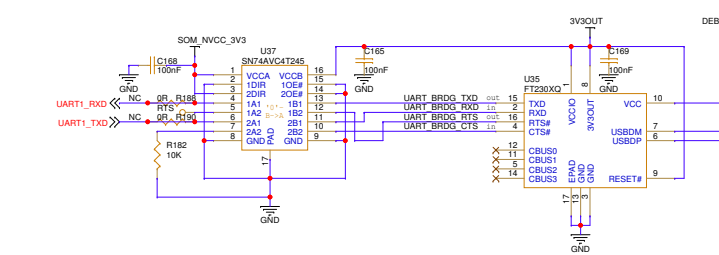
**ASSY NOTE:** Customers requiring PCIe on DT8MP and DT8MM routed to M.2 connector (located on PS) should follow:

Remove C16 C17 C26 C25 R116 R117 C13 C14 R96 R97

Assemble C237 C238 (100nF) C235 C236 (0 Ohm) C233 C234 (0 Ohm) R264 R265 (22 Ohm)

CLK\_REQ\_B path and enable not connected

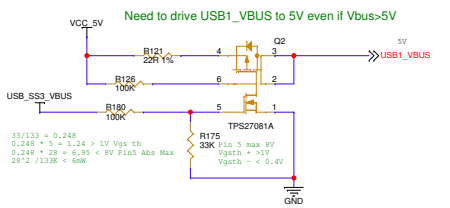
## USB UART DEBUG



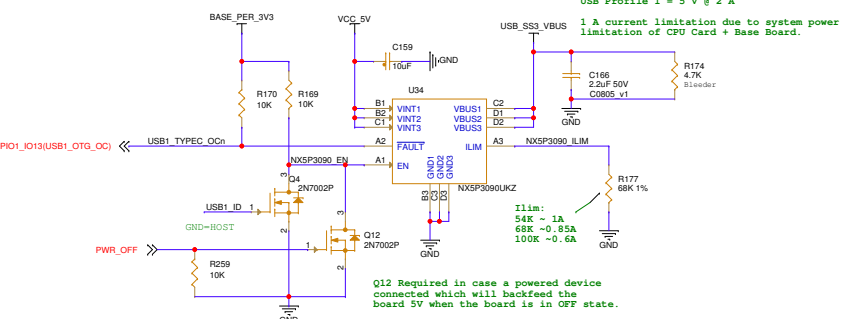
Title: 07. PCIe, QSPI, MIPI-DSI, USB DEBUG			
Size A2	Document Number: VAR-DTBMCustomBoard	Project: VAR-DTBMCustomBoard	Rev: 3.0C R1.7
Designer: Leonid S.	Approved By: -Approved By-	Date: Tuesday, August 05, 2025	Sheet 11 of 17

08. USB TYPE C, USB 3 HUB

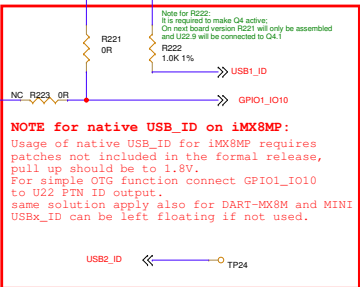
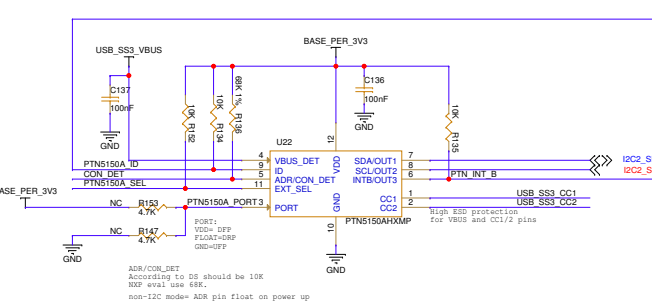
USB#1 - DRP  
USB TYPE C



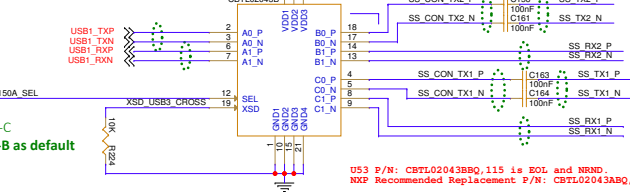
5V Source Load Switch



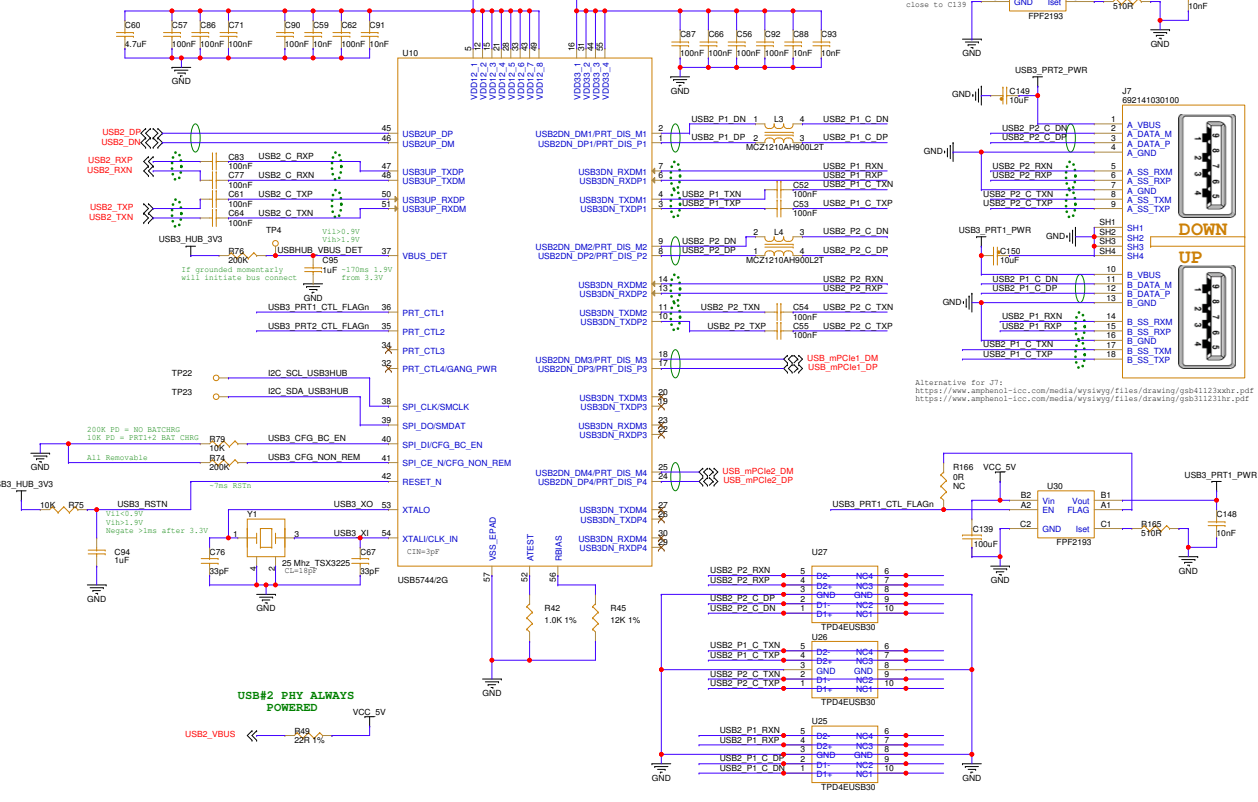
Config Channel Logic Detection & Indication of Plug Orientation



USB3.0 Type-C crossbar switch



USB#2 - HOST  
USB3.0 HUB



Note:  
1.2V should rise before or at the same time as 3.3V  
Straps should be valid >ms after RST\_N negate

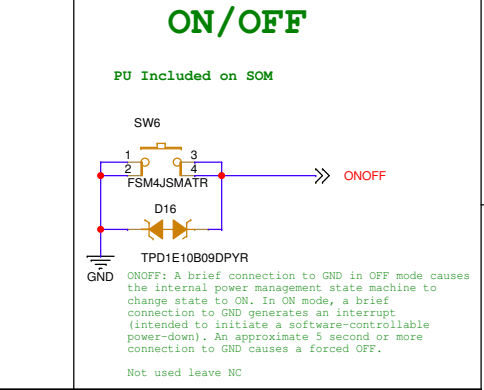
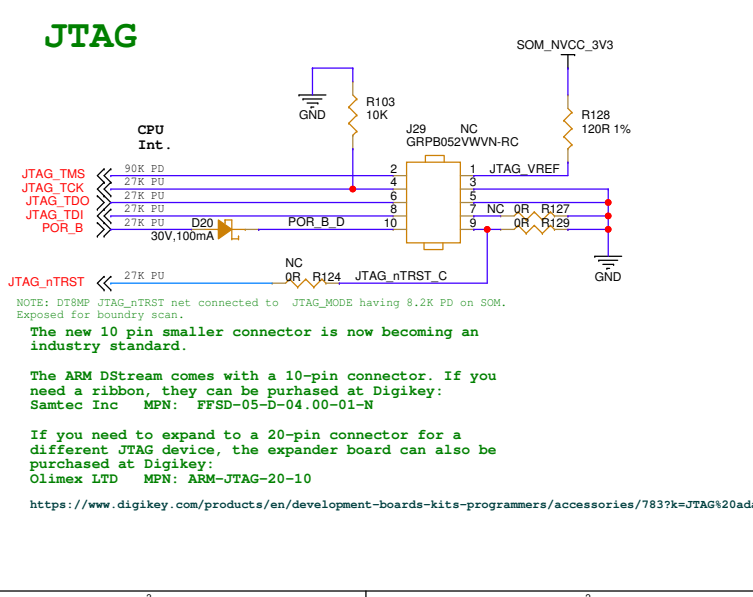
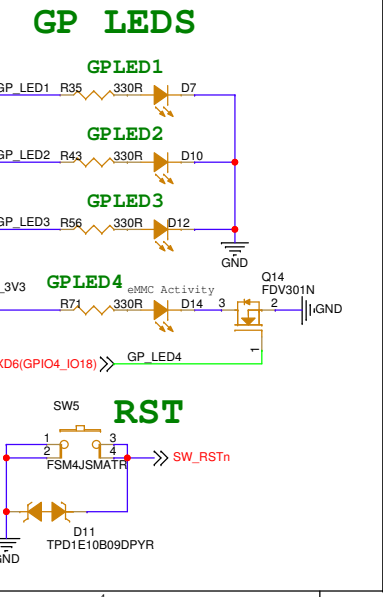
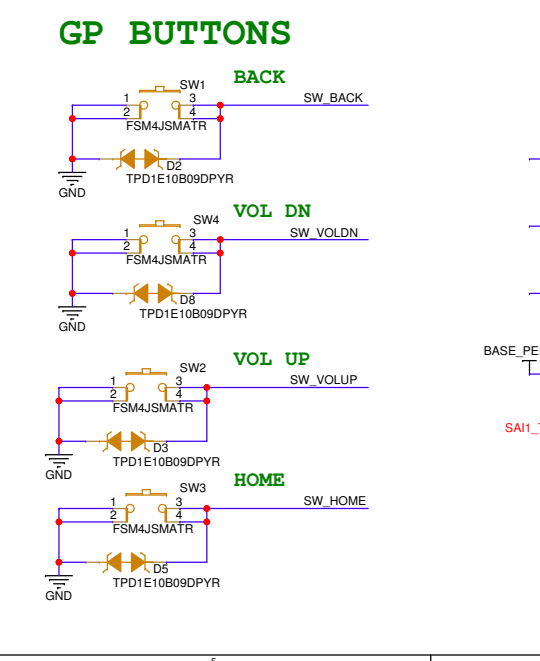
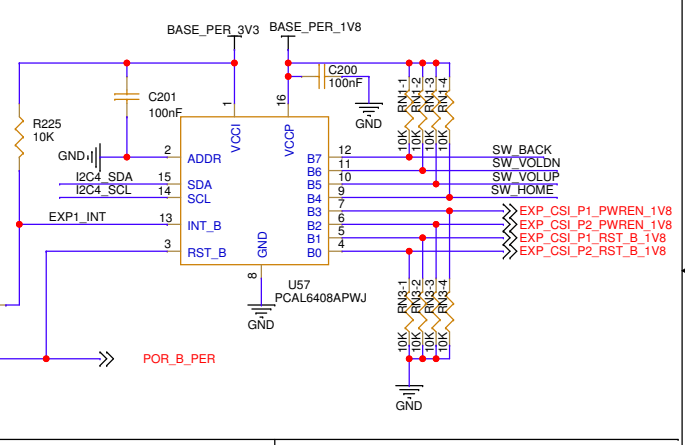
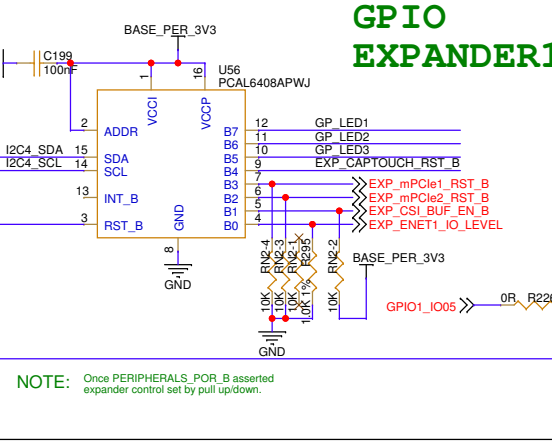
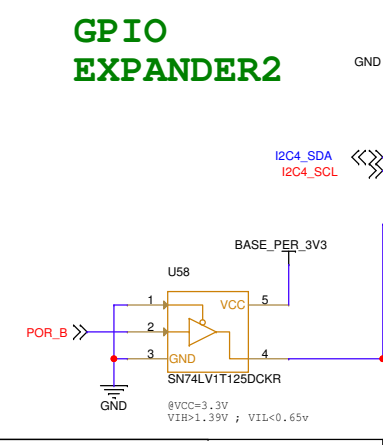
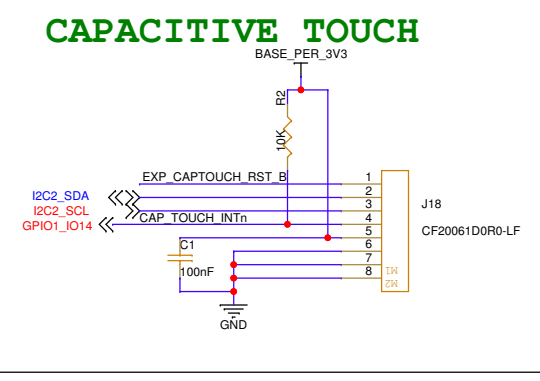
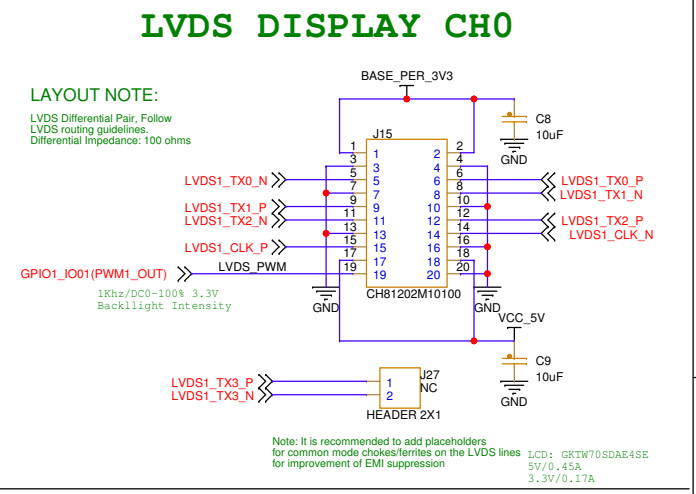
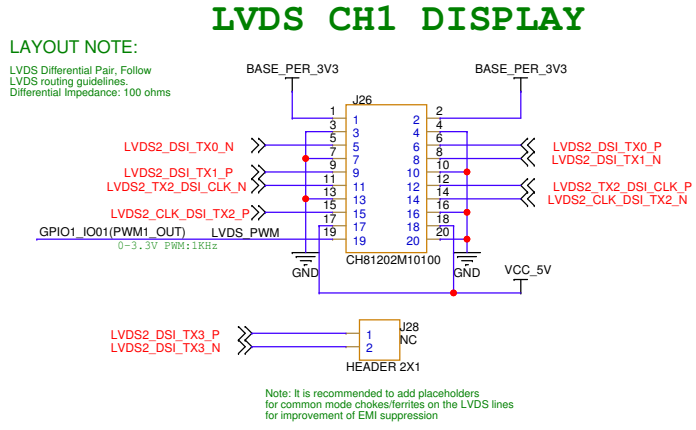
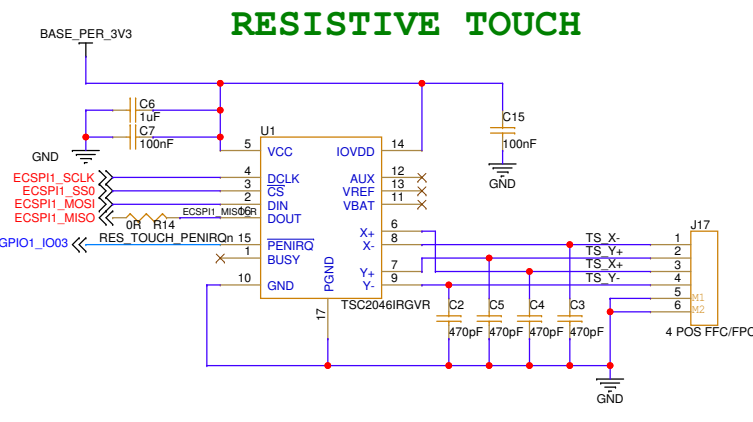
USB#2 PHY ALWAYS POWERED

LAYOUT NOTE:  
USB 2.0 D+ pair, annotated with a ring around the pair.  
USB 3.0 D+ pair annotated with dashed ring  
Follow USB 2.0/3.0 routing guidelines.  
Differential impedance: 90 ohms

Note:  
VBUS active discharge replaced with bleeder

Title: 08. USB TYPE C, USB3 HUB			
Size A2	Document Number: VAR-DT8MCustomBoard	Project: VAR-DT8MCustomBoard	Rev: 3.0C R1.7
Designer: Leonid S.	Approved By:		Sheet 12 of 17
Date: Tuesday, August 05, 2025			

# 09. LVDS, TOUCH, JTAG, I2C EXP



Title: VAR-DT8MCustomBoard

Size A3

Document Number: VAR-DT8MCustomBoard

Project: VAR-DT8MCustomBoard

Rev: 3.0C R1.7

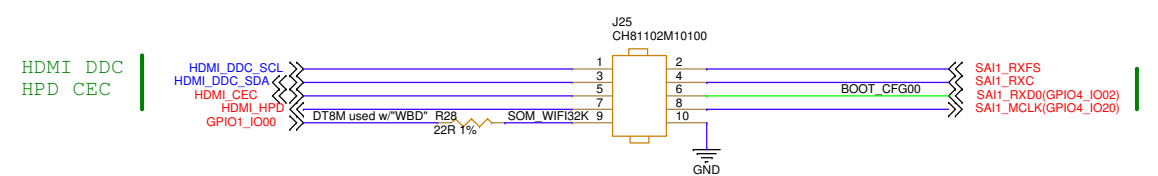
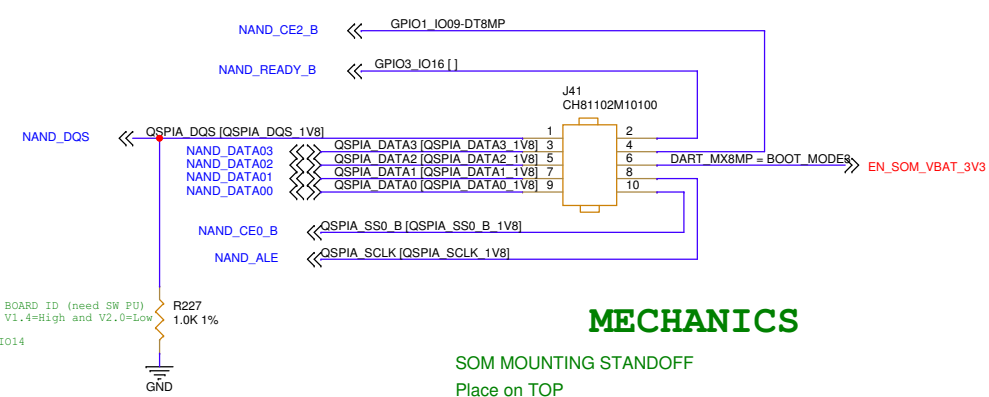
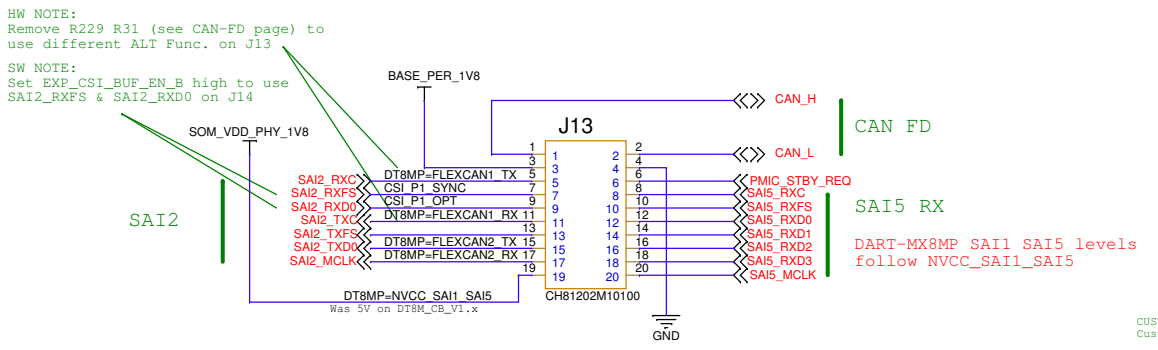
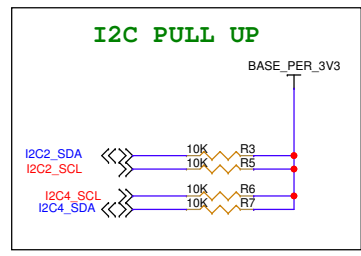
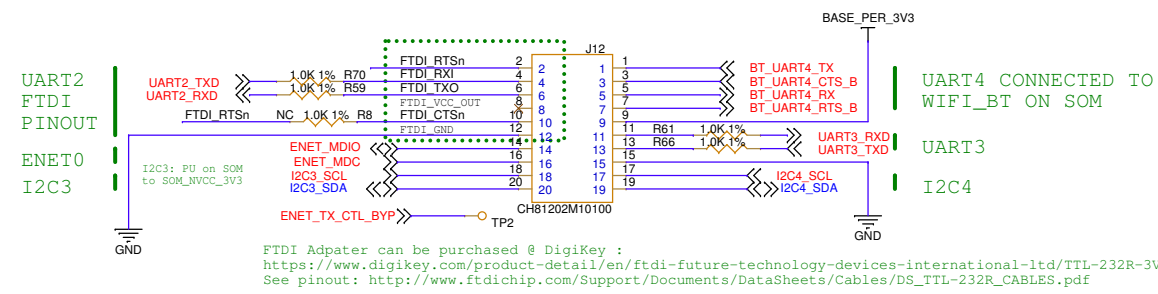
Designer: Leonid S.

Date: Tuesday, August 05, 2025

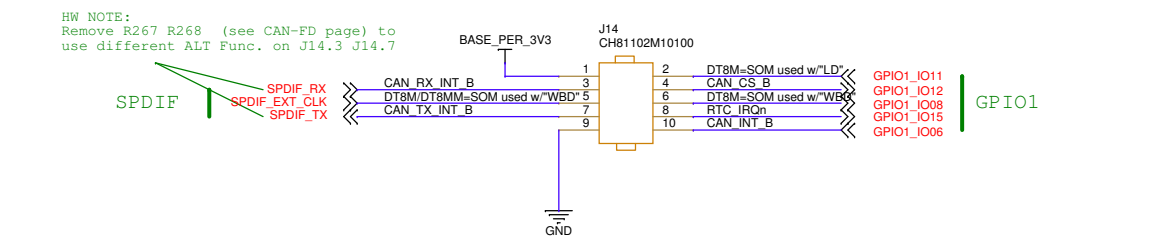
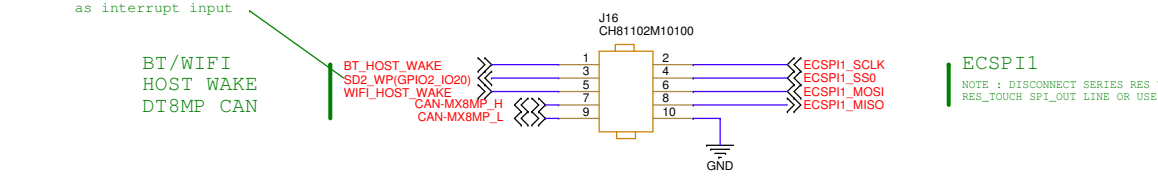
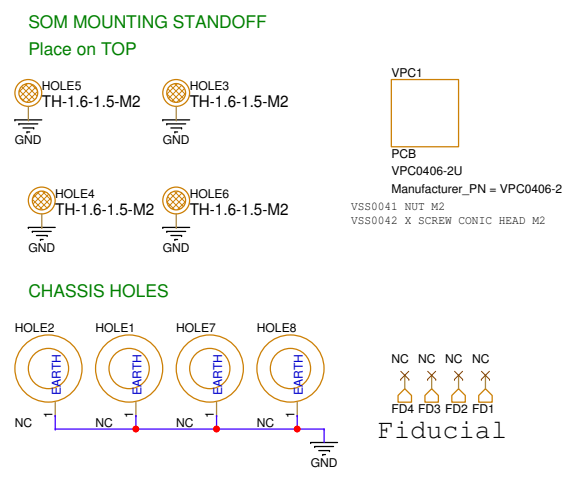
Approved By: [Signature]

Sheet: 13 of 17

# 10. HEADERS, Mechanics, Pull Ups



## MECHANICS



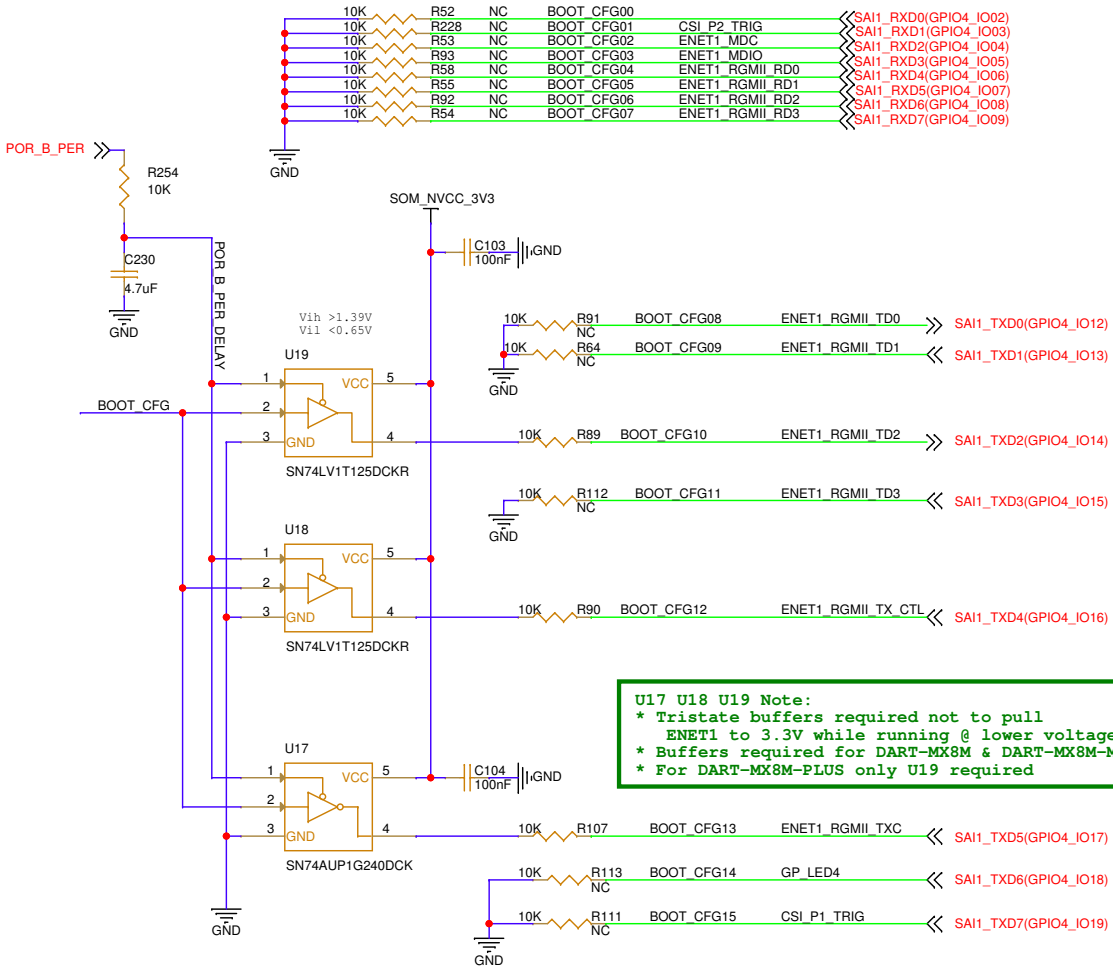
**Variscite**

Title  
10. HEADERS, Mechanics, Pull Ups

Size A3	Document Number VAR-DT8MCustomBoard	Project VAR-DT8MCustomBoard	Rev 3.0C R1.7
Designer Leonid S.	Date Tuesday, August 05, 2025	Approved By	Sheet 14 of 17

# 11. BOOT CONFIG & MODE

		INT. BOOT	EXT. BOOT		
SAI1_RXD0(GPIO4_IO02)	CS1 P2 TRIG	BOOT_CFG00	0	0	Need to Enable PU in DTS; See pp. 5
SAI1_RXD1(GPIO4_IO03)		BOOT_CFG01	0	0	
SAI1_RXD2(GPIO4_IO04)	ENET1 MDC	BOOT_CFG02	0	0	
SAI1_RXD3(GPIO4_IO05)	ENET1 MDIO	BOOT_CFG03	0	0	
SAI1_RXD4(GPIO4_IO06)	ENET1 RGMII RD0	BOOT_CFG04	0	0	
SAI1_RXD5(GPIO4_IO07)	ENET1 RGMII RD1	BOOT_CFG05	0	0	
SAI1_RXD6(GPIO4_IO08)	ENET1 RGMII RD2	BOOT_CFG06	0	0	
SAI1_RXD7(GPIO4_IO09)	ENET1 RGMII RD3	BOOT_CFG07	0	0	
SAI1_TXD0(GPIO4_IO12)	ENET1 RGMII TD0	BOOT_CFG08	0	0	
SAI1_TXD1(GPIO4_IO13)	ENET1 RGMII TD1	BOOT_CFG09	0	0	
SAI1_TXD2(GPIO4_IO14)	ENET1 RGMII TD2	BOOT_CFG10	0	1	
SAI1_TXD3(GPIO4_IO15)	ENET1 RGMII TD3	BOOT_CFG11	0	0	
SAI1_TXD4(GPIO4_IO16)	ENET1 RGMII TX_CTL	BOOT_CFG12	0	1	
SAI1_TXD5(GPIO4_IO17)	ENET1 RGMII TXC	BOOT_CFG13	1	0	
SAI1_TXD6(GPIO4_IO18)	GP_LED4	BOOT_CFG14	0	0	
SAI1_TXD7(GPIO4_IO19)	CSI P1 TRIG	BOOT_CFG15	0	0	



**U17 U18 U19 Note:**  
 \* Tristate buffers required not to pull ENET1 to 3.3V while running @ lower voltage.  
 \* Buffers required for DART-MX8M & DART-MX8M-MINI  
 \* For DART-MX8M-PLUS only U19 required

- Notes:**
- Sampled on rising edge of POR\_B
  - SOC PD during POR\_B and after on BOOT\_CFG[15:0] and BOOTMODE[1:0]
  - BOOT\_MODE[1:0] ="10" is Internal Boot - Always used.
  - Active boot cfg for one dip sw sel EXTERNAL/INTERNAL

**DART-MX8M-MINI Notes:**

- Boot config lines do not follow the Mini datasheet in full  
 DART-MX8M-MINI have added logic to be compatible to DART-MX8M

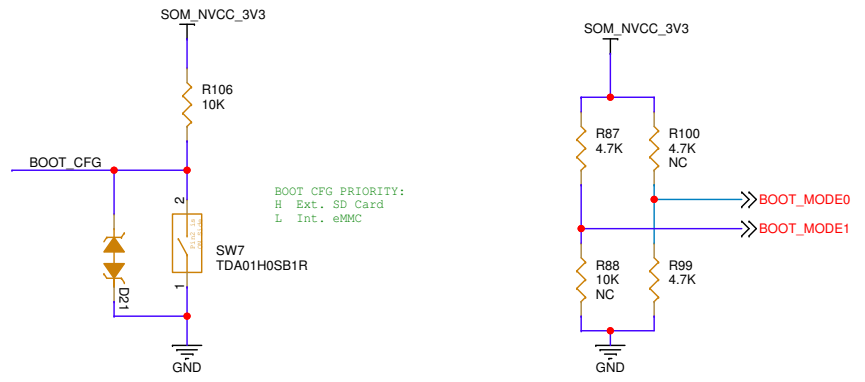
**DART-MX8M-PLUS Notes:**

- Boot configuration set only by SAI1\_TXD2 connected on DART via buffer to BOOT\_MODE0

*i.MX8M Plus Boot Mode*

BOOT_MODE0	BOOT_MODE2	BOOT_MODE1	BOOT_MODE0	Boot Modes
0	0	0	0	Boot From Internal Fuses
0	0	0	1	USB Serial Download
0	0	1	0	USDHC3 (eMMC boot only, SD3 8-bit) Default
0	0	1	1	USDHC2 (SD boot only, SD2)

CustomBoard Net: EN\_SOM\_VBAT\_3V3 BOOT\_MODE0 SAI1\_TXD2 BOOT\_MODE1  
**DART-MX8MP BOOT MODE**



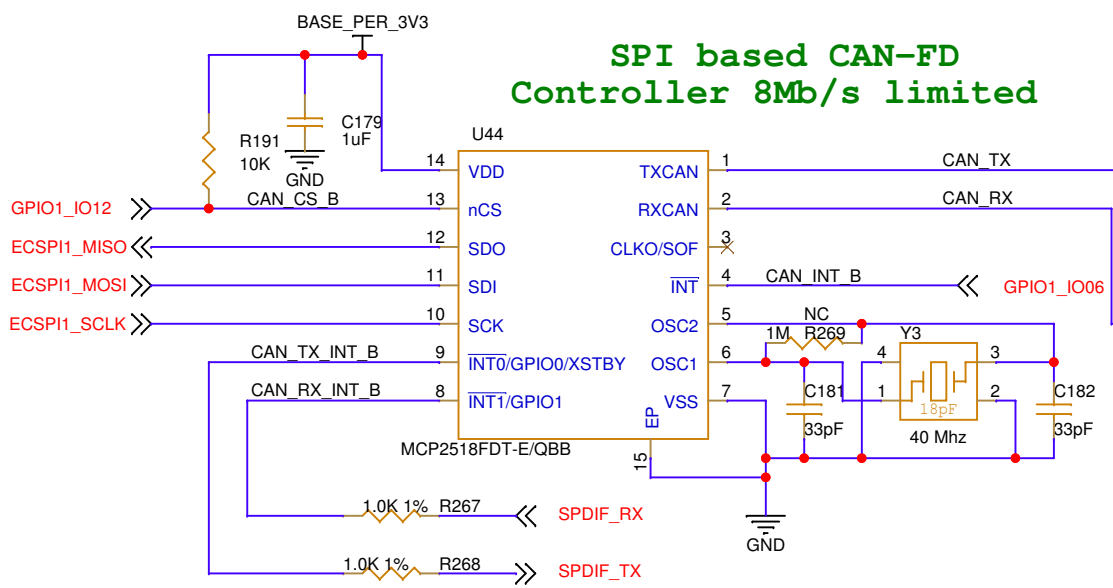
BOOT\_CFG PRIORITY:  
 H Ext. SD Card  
 L Int. eMMC



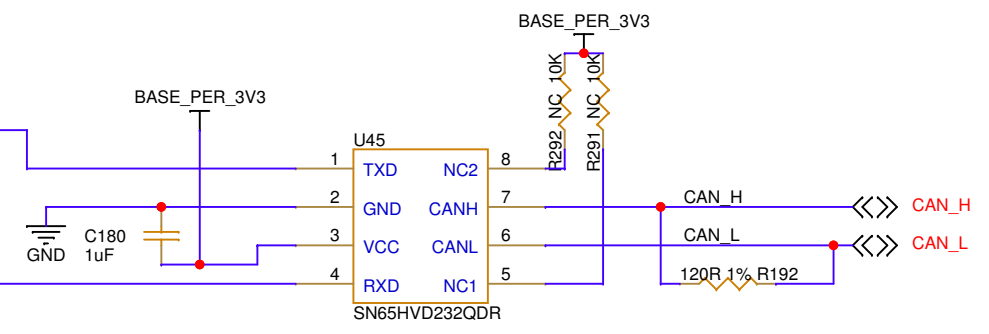
Title 11. BOOT CONFIG & MODE			
Size B	Document Number VAR-DT8MCustomBoard	Project VAR-DT8MCustomBoard	Rev 3.0C R1.7
Designer: Leonid S.	Date: Tuesday, August 05, 2025		Approved By: Sheet 15 of 17

# 13. CAN FD Interface

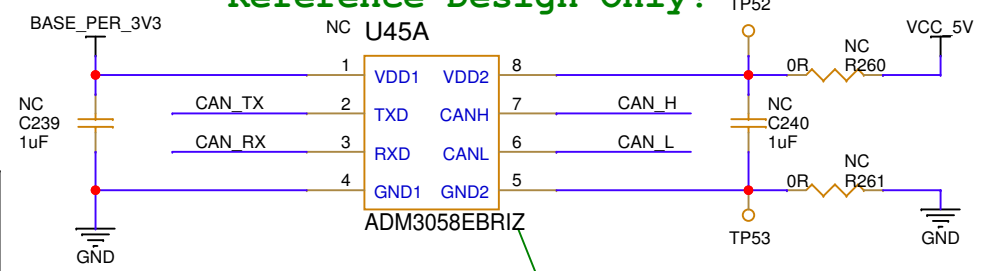
## SPI based CAN-FD Controller 8Mb/s limited



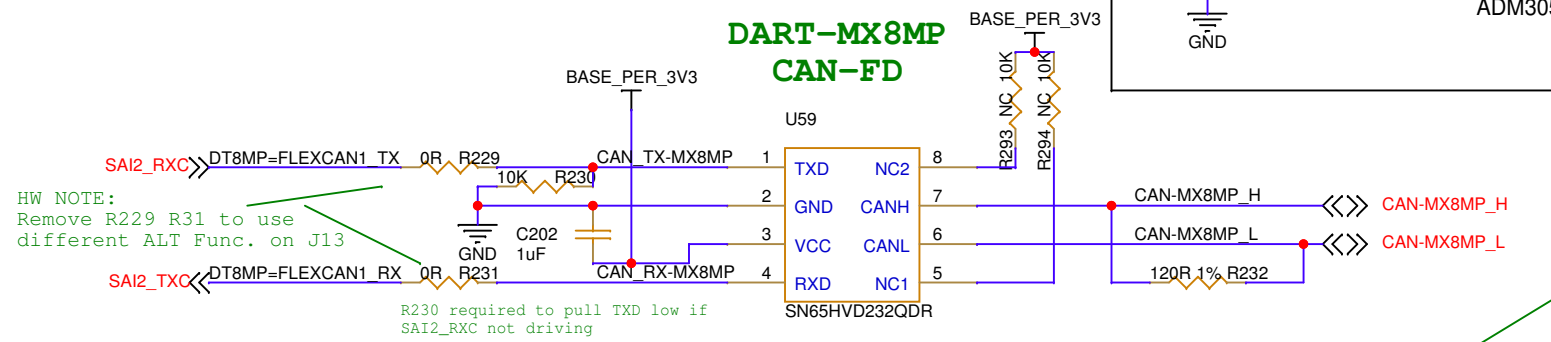
## CAN PHY 5Mb/s Limited



## CAN PHY 12Mb/s Reference Design Only!

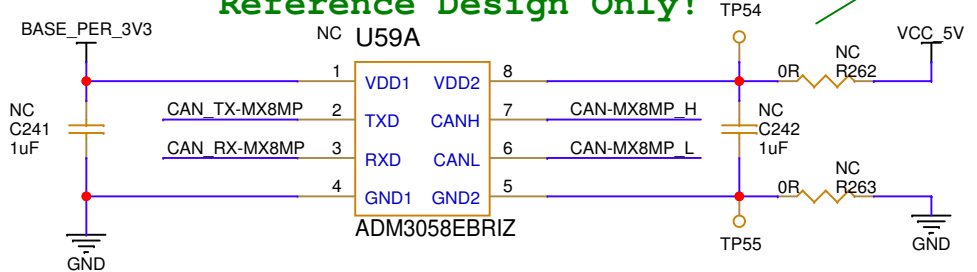


## DART-MX8MP CAN-FD



**NOTE FOR U59A U45A**  
 - Located on bottom side  
 - When assembling the ADM3058E IC removal of TCAN332 is a must!

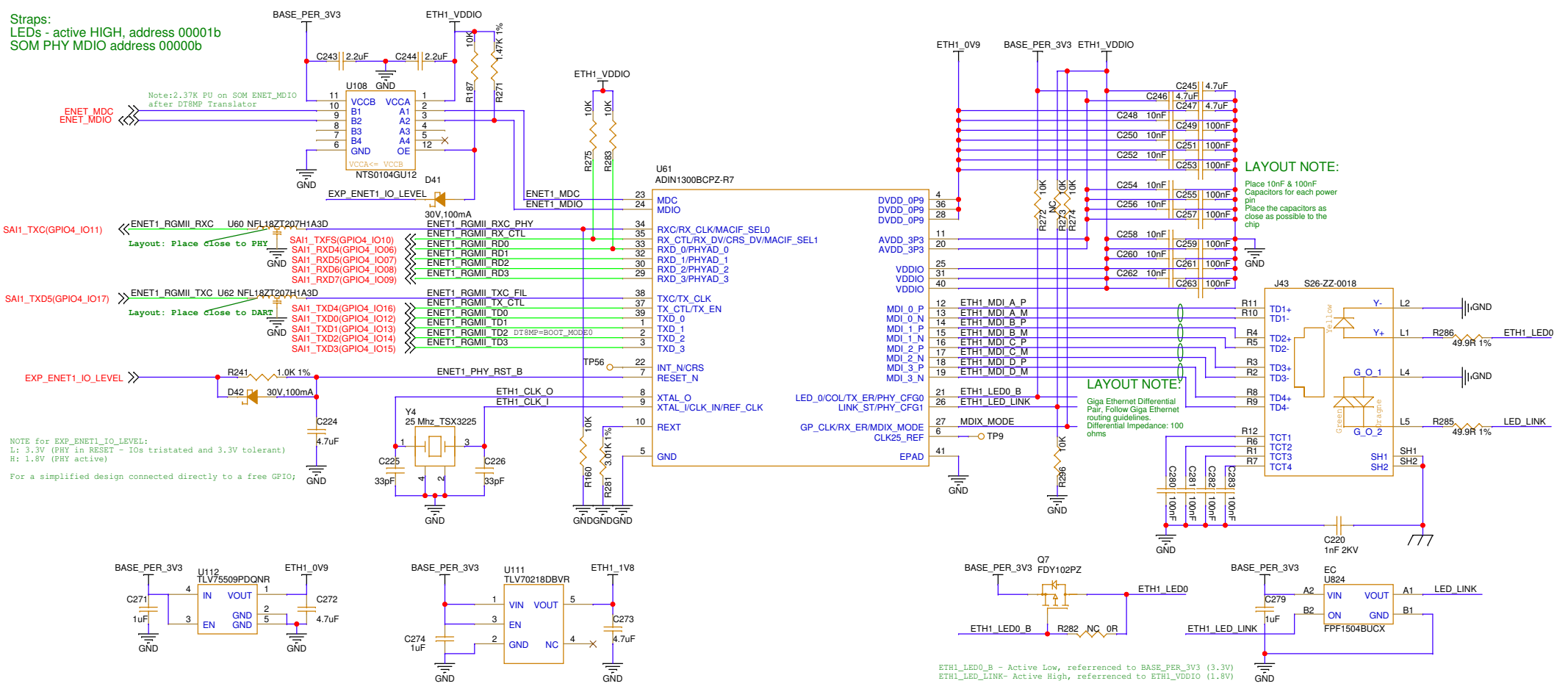
## CAN PHY 12Mb/s Reference Design Only!



Title 12. CAN FD Interface			
Size A4	Document Number VAR-DT8MCustomBoard	Project VAR-DT8MCustomBoard	Rev 3.0C R1.7
Designer: Leonid S.		Approved By:	
Date: Tuesday, August 05, 2025		Sheet 16 of 17	

# 13. DART-MX8MP- ENET1 Gigabit Ethernet

Straps:  
LEDs - active HIGH, address 00001b  
SOM PHY MDIO address 00000b

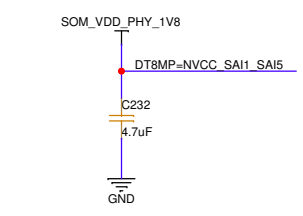


**LAYOUT NOTE:**  
Place 10nF & 100nF Capacitors for each power pin!  
Place the capacitors as close as possible to the chip

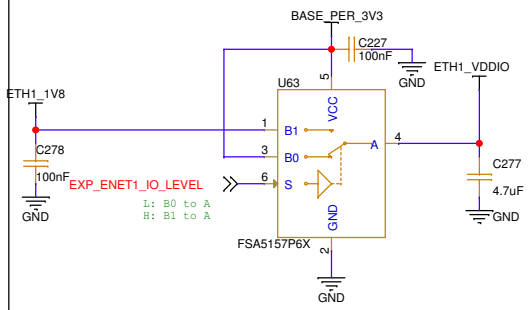
**LAYOUT NOTE:**  
Giga Ethernet Differential Pair. Follow Giga Ethernet routing guidelines.  
Differential Impedance: 100 ohms

NOTE for EXP\_ENET1\_IO\_LEVEL:  
L: 3.3V (PHY in RESET - IOs tristated and 3.3V tolerant)  
H: 1.8V (PHY active)  
For a simplified design connected directly to a free GPIO;

**NOTE:**  
For DT8MP net SOM\_VDD\_PHY\_1V8 connected to NVCC\_SAI1\_SAI5 which is an output from the DT8MP programmable PMIC LDO.  
This output voltage will set SAI1 and SAI5 pads voltage level; With DT8MCustomBoard-V1.x and earlier it is set to 3.3V. On DT8MCustomBoard-V2.x it is set to 1.8V for RGMII.  
Bypass with 4.7uF min. 6.3V capacitor.



**NOTE for U63:**  
Required for compatibility to DT8M & DT8MM where SAI1 levels are fixed to 3.3V;



**NOTE:**  
Test points below used to access DT8M & DT8MM SAI1 signals;  
Levels are fixed to 3.3V by modules;

- SAI1\_RXD2(GPIO4\_I004) >>> DT8MP-ENET1\_MDC TP50
- SAI1\_RXD3(GPIO4\_I005) >>> DT8MP-ENET1\_MDIO TP51
- SAI1\_RXD4(GPIO4\_I006) >>> ENET1\_RGMII\_RD0 TP31
- SAI1\_RXD5(GPIO4\_I007) >>> ENET1\_RGMII\_RD1 TP33
- SAI1\_RXD6(GPIO4\_I008) >>> ENET1\_RGMII\_RD2 TP37
- SAI1\_RXD7(GPIO4\_I009) >>> ENET1\_RGMII\_RD3 TP35
- SAI1\_TXC(GPIO4\_I011) >>> ENET1\_RGMII\_RXC TP40
- SAI1\_TXFS(GPIO4\_I010) >>> ENET1\_RGMII\_RX\_CTL TP41
- SAI1\_TXD0(GPIO4\_I012) >>> ENET1\_RGMII\_TD0 TP32
- SAI1\_TXD1(GPIO4\_I013) >>> ENET1\_RGMII\_TD1 TP34
- SAI1\_TXD2(GPIO4\_I014) >>> ENET1\_RGMII\_TD2 TP38
- SAI1\_TXD3(GPIO4\_I015) >>> ENET1\_RGMII\_TD3 TP39
- SAI1\_TXD5(GPIO4\_I017) >>> ENET1\_RGMII\_TXC TP36
- SAI1\_TXD4(GPIO4\_I016) >>> ENET1\_RGMII\_TX\_CTL TP42



Title 13. Ethernet2			
Size A3	Document Number VAR-DT8MCustomBoard	Project VAR-DT8MCustomBoard	Rev 3.0C R1.7
Designer Leonid S.	Date Tuesday, August 05, 2025	Approved By	Sheet 17 of 17